4460 73096

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Date 8/12/02 Serial # 10/013,103 Priority Application Date 6/26/98

Your Name Milewois Examiner #

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In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other:

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ___

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 17-24

Problem: See Page 2 lines 6-26
3 " 1-6

Solution: " " 4 " 1-6
novelty in the structure of the claims

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Searcher: Derrick Blalock

Searcher Phone:

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 8/13/02

Date Completed: 8/14/02

Searcher Prep/Rev Time: 230

Online Time: 101

Type of Search

Structure (#)

Bibliographic ✓

Litigation

Fulltext

Patent Family

Other

Vendors

STN ✓

Dialog ✓

Questel/Orbit

Lexis-Nexis

WWW/Internet

Other

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     FILE 'REGISTRY' ENTERED AT 15:46:11 ON 13 AUG 2002
                  E O2 SI/MF
L1            47 S E3
                  E SILICON OXYNITRIDE/CN
                  E E3
L2             2 S E3
                  E O2 N2 SI/MF
                  E N2 O2 SI/MF
L3             1 S E3
                  E N4SI3/MF
L4             3 S E3
L5         46646 S PI/PCT

     FILE 'HCAPLUS' ENTERED AT 16:01:37 ON 13 AUG 2002
L6        231172 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(
L7        815472 S (SILICON OR SI)()(DIOXIDE OR O2) OR SILICA## OR SILICATE OR K
L8          4507 S (SILICON OR SI)()(OXYNITRIDE) OR DISILICON OXYNITRIDE OR SILI
L9         69894 S (SILICON OR SI3)()(NITRIDE OR N4) OR SI3N4 OR BAYSINID OR DEN
L10       247552 S (INSULAT? OR OXIDE OR DIELECTRIC)(2N)(LAYER? OR FILM OR COAT#
L11      2373522 S ADHESI? OR ADHERE? OR STICK? OR CLING? OR BOND? OR CEMENT? OR
L12        52375 S L10 AND (L1 OR L7)
L13          858 S L11 AND (L2 OR L8 OR L3)
                  E PASSIVATION/CT
                  E E3+ALL/CT
L14         2343 S PASSIVAT? AND (L4 OR L9)
                  E POLYIMIDE/CT
                  E POLYIMIDES/CT
                  E E3+ALL/CT
L15         7760 S L6 AND L12
L16           54 S L15 AND L13
L17          184 S L15 AND L14
L18           14 S L16 AND L14
L19           16 S L16 AND PASSIVAT?
L20            2 S L19 NOT L18
L21         2901 S L1 AND PASSIVAT?
L22         2901 S L21 AND (L1 OR L7)
L23          130 S L21 AND (L2 OR L8 OR L3)
L24          121 S L23 AND (L4 OR L9)
L25           86 S L24 AND L10
L26           21 S L25 AND L11
L27            8 S L26 NOT (L18 OR L19)
L28         2984 S L1 AND (L1 OR L7) AND (L2 OR L8 OR L3) AND (L4 OR L9)
L29          100 S L28 AND (L5 OR POLYIMIDE)
L30           19 S L29 AND PASSIVAT?
L31           14 S L30 NOT (L18 OR L19 OR L26)
                  E SESHAN KRISHNA/AU
L32           14 S E3
                  E SESHAN K/AU
L33          164 S E3-5
L34            0 S DASS M. LAWRENCE/AU
                  E DASS M. LAWRENCE/AU
L35            1 S E1
                  E DASS M L/AU
L36           21 S E3-6
                  E BAKKER GEOFFREY L/AU
L37            5 S E3
                  E BAKKER G L/AU
L38            6 S E3
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L39	205	S L32-38
L40	6	S L39 AND L1
L41	5	S L40 NOT (L30 OR L18 OR L19 OR L26)

L20 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:401809 HCAPLUS
DN 136:378298
TI Isolated protection process of the copper metal layer with liner layer and etching stop layer
IN Liou, Jung-Shi; Yu, Jen-Hua
PA Taiwan Semiconductor Mfg Co. Ltd., Taiwan
SO Taiwan, 11 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 406139	B	20000921	TW 1999-88102268	19990212

AB This invention provides an isolated protection process of the Cu metal, which comprises the steps of: (a) providing a semiconductor substrate having a Cu metal layer thereon; (b) forming a liner layer and a etching stop layer on the Cu metal layer sequentially, in which the **adhesion** of the liner layer toward the Cu is better than that of the etching stop layer; and (c) depositing an inter metal dielecs. or a **passivation** layer on the etching stop layer. This invention solves the problem of poor **adhesion** between the etching stop layer (such as SiON) and the Cu metal, and maintains excellent etching stop ability on the same time.

L20 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:630926 HCAPLUS
DN 135:188774
TI **Integrated circuit** with improved **adhesion** between interfaces of conductive and dielectric surfaces
IN Ngo, Minh Van; Huang, Richard J.; Morales, Guarionex
PA Advanced Micro Devices, Inc., USA
SO U.S., 9 pp., Cont.-in-part of U.S. 6,252,303.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6281584	B1	20010828	US 1999-373482	19990812
	US 6252303	B1	20010626	US 1998-203572	19981202
PRAI	US 1998-203572	A2	19981202		

AB A method for using low dielec. SiOF in a process to manuf. semiconductor products, comprising the steps of obtaining a layer of SiOF, and depleting F from a surface of the SiOF layer. In a preferred embodiment, the depleting step comprises the step of treating the surface of the layer of SiOF with a plasma contg. NH_3. It is further preferred that the treated surface be **passivated** by a nitrite plasma. The invention also encompasses a semiconductor **chip** comprising an **integrated circuit** with at least a 1st and 2nd layers, and with a dielective layer of SiOF disposed between the layers, in which the SiOF **dielec. layer** includes a 1st region at 1 edge thereof which is depleted of F to a predetd. depth.

L18 ANSWER 1 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:483055 HCAPLUS
DN 137:40326
TI Process for fabricating copper interconnect for ULSI **integrated circuits**
IN Ryan, Vivian W.
PA Agere Systems Guardian Corp., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6410435	B1	20020625	US 1999-410686	19991001

AB A method is claimed for fabricating copper interconnects with better resistance to electromigration, improved wire **bonding**, and storage capability. A method for manufg. **integrated circuits** is claimed, particularly, a method for fabricating a Cu interconnect system and a Cu interconnect system, having a layer of CrO, fabricated by the method.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 2 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:214949 HCAPLUS
DN 136:255665
TI Methods for making interconnects and diffusion barriers in **integrated circuits**
IN Dubin, Valery
PA Intel Corporation, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6359328	B1	20020319	US 1998-224941	19981231
	US 2002094673	A1	20020718	US 2002-93898	20020308
PRAI	US 1998-224941	A3	19981231		

AB The inventor devised methods of forming interconnects that result in conductive structures with fewer voids and thus reduced elec. resistance. One embodiment of the method starts with an **insulative layer** having holes and trenches, fills the holes using a selective electroless deposition, and fills the trenches using a blanket deposition. Another embodiment of this method adds an anti-**bonding** material, such as a surfactant, to the metal before the electroless deposition, and removes at least some the surfactant after the deposition to form a gap between the deposited metal and interior sidewalls of the holes and trenches. The gap serves as a diffusion barrier. Another embodiments leaves the surfactant in place to serve as a diffusion barrier. These and other embodiments ultimately facilitate the speed, efficiency, or fabrication of **integrated circuits**.
RE.CNT 59 THERE ARE 59 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:213782 HCAPLUS
DN 136:240141
TI Method for forming a top metal interconnection level and **bonding** pads on a multilevel **integrated circuit chip**
IN Liu, Meng-Chang; Liu, Yuan-Lung
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6358831	B1	20020319	US 1999-261680	19990303

AB A method for forming a top interconnection level and **bonding** pads for a multilevel **integrated circuit chip** is described. The interconnection level is formed by a damascene type process. **Bonding** pads are placed above the plane of the wiring channels of the interconnection level. This eliminates the problem of dishing of the relatively large **bonding** pads which occurs, during chem. mech. polishing, when the **bonding** pads are on the same level as the interconnection metallurgy. The interconnection wiring includes a smaller pad base segment upon which the larger **bonding** pad is then formed. The **bonding** pad base segments are small enough that dishing during CMP is not a problem. Placing the **bonding** pads on pad bases provides for a more robust pad. The top level and **bonding** pad fabrication procedures are applicable with various conductive materials including Al, W, and Cu.
RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:163838 HCAPLUS
DN 136:209188
TI **Passivation** deposition process for improving interfacial **adhesion** between oxide and hard **passivation** layers to prevent delamination in **integrated circuits**
IN Seshan, Krishna; Dass, M. Lawrence A.; Bakker, Geoffrey L.
PA Intel Corporation, USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6352940	B1	20020305	US 1998-105590	19980626

AB A method of **passivating** an **integrated circuit** (**IC**) is provided. An **insulating layer** is formed onto the **IC**. An **adhesion** layer is formed onto a surface of the **insulating layer** by treating the surface of the **insulating layer** with a gas and gas plasma. A 1st **passivation** layer is formed upon the **adhesion** layer, the 1st **passivation** layer and the gas and gas plasma including at least one common chem. element.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:851543 HCAPLUS
DN 135:379714
TI Encapsulated **microelectronic** devices
IN Graff, Gordon Lee; Martin, Peter Maclyn; Gross, Mark Edward; Shi, Ming Kun; Hall, Michael Gene; Mast, Eric Sidney
PA Battelle Memorial Institute, USA
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001089006	A1	20011122	WO 2001-US6562	20010301

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI US 2000-571649 A 20000515
AB An encapsulated **microelectronic** device. The device includes a semiconductor substrate, **microelectronic** device adjacent to the semiconductor substrate, and .gtoreq.1 1st barrier stack adjacent to the **microelectronic** device. The barrier stack encapsulates the **microelectronic** device. It includes .gtoreq.1 1st barrier layer and .gtoreq.1 1st polymer layer. The encapsulated **microelectronic** device optionally includes .gtoreq.1 2nd barrier stack located between the semiconductor substrate and the **microelectronic** device. The 2nd barrier stack includes .gtoreq.1 2nd barrier layer and .gtoreq.1 2nd polymer layer. A method for making an encapsulated **microelectronic** device is also disclosed.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:703763 HCAPLUS
DN 135:235008
TI Process for controlling oxide thickness over a fusible link using transient etch stops
IN Tzeng, Wen-Tsing; Chen, Yue-Feng; Wang, Kau-Jan
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6294474	B1	20010925	US 1999-425906	19991025

AB A method is described for progressively forming a fuse access opening for laser trimming in an **integrated circuit** with improved control of dielec. thickness over the fuse. A **dielec. layer** is formed over the fuse and a polysilicon layer is then patterned over the fuse to form a 1st etch stop. An inter-level

dielec. (ILD) **layer** is added and a 2nd etch stop is formed in a 1st metal layer on the ILD layer over the 1st etch stop. The 2nd etch stop serves to protect the ILD layer over the fuse from being etched by an ARC over etch during the via etching in a 1st inter-metal **dielec**. (IMD) **layer**. A 1st portion of the laser access window is formed during the via etching of the 1st IMD layer. The 2nd etch stop is then removed by the 2nd metal patterning etch, exposing the ILD layer over the 1st etch stop at it's original thickness. A **passivation** layer is deposited and patterned to form access openings to **bonding** pads as well as to further open the laser access window to the 1st etch stop. The 1st etch stop prevents penetration of the subjacent **insulative layer** over the fuse, thereby maintaining a controlled uniform thickness of that layer. When the **bonding** pads are opened, including the removal of an ARC on their surface, the etchant conditions are changed to remove the etch stop and subsequently a portion of the subjacent **insulative layer** over the fuse leaving a precise and uniform thickness of dielec. material over the fuse. The process fits conveniently within the framework of an existing process and does not introduce any addnl. steps.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:592239 HCAPLUS
DN 135:161027
TI HDP-CVD method for forming **passivation** layers with enhanced **adhesion** for semiconductor devices
IN Jang, Syun-Ming; Fu, Chu-Yun
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6274514	B1	20010814	US 1999-336807	19990621

AB A method is presented for forming upon a substrate employed within a **microelectronics** fabrication a **dielec**. **passivating layer** with attenuated delamination and improved **adhesion** to subsequent **passivating** and encapsulating materials. A substrate is provided to be employed within a **microelectronics** fabrication. On the substrate a patterned **microelectronics** layer is formed. Over the substrate a Si contg. **dielec**. **layer** is formed, employing high d. plasma CVD (IDP-CVD) in 2 steps, in which the conditions of the HDP-CVD process are optimized during the 2nd step to provide a final layer portion with a greater degree of surface topog. Subsequently, an addnl. **passivation** layer is formed over the substrate with attenuated delamination and an org. polymer overcoat layer with improved **adhesion**.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 8 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:186063 HCAPLUS
DN 134:201658
TI Strongly textured atomic ridges and dots in a MOSFET device
IN Kendall, Don; Guttag, Mark

PA Starmega Corporation, USA
SO PCT Int. Appl., 69 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001018866	A1	20010315	WO 2000-US24815	20000908

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	US 6413880	B1	20020702	US 2000-657533	20000908
	EP 1221179	A1	20020710	EP 2000-966708	20000908

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL

PRAI	US 1999-153088P	P	19990910
	WO 2000-US24815	W	20000908

AB The present invention provides a MOSFET device comprising: a substrate including a plurality of at. ridges, each of the at. ridges including a semiconductor layer comprising Si and a **dielec. layer** comprising a Si compd.; a plurality nanogrooves between the at. ridges; .gtoreq.1 elongated mol. located in .gtoreq.1 of the nanogrooves; a porous gate layer located on top of the plurality of at. ridges. The present invention also provides a membrane comprising: a substrate; and a plurality of nanowindows in the substrate and a method for forming nanowindows in a substrate. The present invention also provides a multi-tip array device comprising: a substrate; a multi-tip array of at. tips on the substrate, the multi-tip array having a pitch of 0.94-5.4 nm between adjacent tips in .gtoreq.1 direction; and means for moving the substrate. The present invention also provides an at. claw comprising: a mounting block; a paddle having a multi-tip array thereon, the multi-tip array having a pitch of 0.94-5.4 nm between adjacent tips in .gtoreq.1 direction; and a cantilever connected to the paddle and the mounting block, in which the cantilever allows the paddle to be moved in .gtoreq.1 arcuate direction.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:131180 HCAPLUS
DN 134:156520
TI Improving copper pad **adhesion** in fabricating an **integrated circuit**
IN Chen, Sheng-hsiung
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

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PI   US 6191023        B1   20010220      US 1999-442497   19991118
     US 2001016415     A1   20010823      US 2001-755282   20010108
PRAI US 1999-442497    A3   19991118
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AB This invention relates to a new improved method and structure in the fabricating of Al metal pads. The formation special Al **bond** pad metal structures are described which improve **adhesion** between the Ta nitride pad barrier layer and the underlying Cu pad metallurgy by a special interlocking **bond** pad structure. It is the object of the present invention to provide a process wherein a special grid of interlocking via structures is placed in between the underlying Cu pad metal and the top Ta nitride pad barrier layer providing improved **adhesion** to the Al pad metal stack structure. This unique contact **bond** pad structure provides for thermal stress relief, improved wire **bond adhesion** to the Al pad, and prevents peeling during wire **bond adhesion** tests.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73502 HCAPLUS
DN 134:124771
TI **Passivation** layer etching process for memory arrays with fusible links
IN Tzeng, Wen-Tsing; Yang, Chun-Pin; Lin, Hsing-Lien
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6180503	B1	20010130	US 1999-354852	19990729

AB A method is described for progressively forming a fuse access openings in **integrated circuits** which are built with redundancy and use laser trimming to remove and insert circuit sections. The fuses are formed in a polysilicon layer and covered by .gtoreq.1 relatively thin **insulative layers**. An etch stop is patterned over the fuse in a higher level polysilicon layer or a 1st metalization layer. Addnl. **insulative layers** such as inter-metal **dielec. layers** are then formed over the etch stop. A 1st portion of the laser access window is then etched during the via etch for the top metalization level. The etch stop prevents removal of the insulation subjacent to it. Cumulative thickness non-uniformities in the relatively thick upper **insulative layers** are thus removed from the fuse window. The etch stop is removed during patterning of the top level metalization. A **passivation** layer is applied and patterned to exposed **bonding** pads and, at the same time complete the etching of the laser access window to a desired thickness over the fuses. The **passivation** layer over etch required to penetrate the **insulation layer** over the fuses also removes an antireflective coating over the **bonding** pads. The process fit conveniently within the framework of an existing process and does not introduce any addnl. steps. In addn., the **passivation** layer can be patterned to form final access to both **bonding** pads and laser access openings with a single photolithog. mask.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:794235 HCAPLUS
DN 132:43662
TI Damage-free **passivation** layer etching process
IN Chen, Sen-Fu; Wu, Jie-Shing; Chen, Fang-Cheng; Lee, Tsung-Tser
PA Taiwan Semiconductor Manufacturing Company Ltd., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6001538	A	19991214	US 1998-55442	19980406

AB A method for etching **bonding**-pad-access openings in a **passivation** layer of an **integrated circuit** is described. The method utilizes a two-step etching process wherein a first step etches isotropically through a major portion of the **passivation** layer under conditions which provide very high etching rate selectivities of the **passivation** layer to a photoresist. These high selectivities result in virtually no erosion of the photoresist while the greater part of the openings is etched. A second anisotropic etching step wherein the base of the openings is defined faithfully replicates the dimensions of the mask pattern. The two-step etching process permits the use of a photoresist of a moderate thickness as well as that with thin regions. The minimal erosion of the photoresist during the isotropic etching step secures sufficient photoresist coverage in the thin regions to prevent penetration and attack of **passivation** over wiring lines in the uppermost wiring level of the **integrated circuit**.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:468525 HCAPLUS
DN 131:96168
TI A novel **passivation** structure and its method of fabrication for **integrated circuits**
IN Bohr, Mark T.
PA Intel Corporation, USA
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9934442	A1	19990708	WO 1998-US26689	19981215

W: AL, AM, AT, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ, DE, DE, DK, DK, EE, EE, ES, FI, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	US 6143638	A	20001107	US 1997-1551	19971231
	US 2002064929	A1	20020530	US 1998-115418	19980714

	AU 9919172	A1	19990719	AU 1999-19172	19981215
	JP 2002500445	T2	20020108	JP 2000-526974	19981215
PRAI	US 1997-1551	A	19971231		
	WO 1998-US26689	W	19981215		

AB A novel **passivation** structure and its method of fabrication. According to the present invention a 1st **dielec. layer** (204) is formed upon a conductive layer formed over a substrate. The 1st **dielec. layer** (204) and the conductive layer are then patterned into a 1st dielec. capped interconnect (208) and a dielec. capped **bond** pad (206). Next, a 2nd **dielec. layer** is formed over and between the dielec. capped interconnect (206) and the dielec. capped **bond** pad (208). The top portion of the 2nd **dielec. layer** is removed so as to expose the dielec. capped **bond** pad (208) and the dielec. capped interconnect (206). A 3rd **dielec. layer** (218) is then formed over the exposed dielec. capped **bond** pad and the exposed dielec. capped interconnect and over the 2nd dielec.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:56358 HCAPLUS
DN 130:103828
TI Plated nickel-gold/dielectric interface for **passivated** MMICs
IN Wen, Cheng P.; Wong, Wah S.; Arthur, Arlene E.
PA Raytheon Company, USA
SO U.S., 4 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5861341	A	19990119	US 1996-680453	19960715

AB A thin film (at least one at. layer to .apprx.400 .ANG.) of Ni is electrolytically plated on top of electrolytically-plated Au electrodes in GaAs monolithic microwave **integrated circuits** (MMICs) without any addnl. photoresist masking step. The thin electrolytically-plated Ni film improves **adhesion** of a **passivating dielec. layer** (e.g., **SiO2**, Si nitride, and **Si oxynitride**) formed on the electrolytically-plated Au electrodes. The electrolytically-plated Ni film can be removed locally to facilitate the fabrication of plated Ag bumps (for off-**chip** elec. connections and thermal paths) on **passivated** flip **chip** MMICs.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:523113 HCAPLUS
DN 121:123113
TI Hermetic protection for **integrated circuits**, based on a ceramic layer
IN Camilletti, Robert Charles; Chandra, Grish; Loboda, Mark Jon; Michael, Keith Winton; Sierawski, David Alan
PA Dow Corning Corp., USA
SO Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 590780	A1	19940406	EP 1993-306587	19930819
	EP 590780	B1	19970625		
	R: DE, FR, GB, IT, NL, SE				

PRAI US 1992-936475 19920828
OS MARPAT 121:123113
AB The circuits are hermetically sealed by applying a non-corroding, conductive layer to the **bond** pads and addnl. ceramic layers to the primary **passivation**.

L27 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:587052 HCAPLUS
DN 133:171066
TI **Passivation** method for copper damascene process in device fabrication
IN Liu, Chung-Shi; Yu, Chen-Hua
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6107188	A	20000822	US 1999-374309	19990816

AB A composite **dielec**. **layer** and method of forming the composite **dielec**. **layer** for the **passivation** of exposed Cu in a Cu damascene structure are described. The composite layer consists of a **passivation dielec**. **layer** and an etch stop **dielec**. **layer** and is formed over the exposed Cu prior to the deposit of an inter-metal or final **passivating dielec**. **layer**. Via holes are etched in the inter-metal or final **passivating** layer and the composite **dielec**. **layer** provides an etch stop function as well as **passivation** for the exposed Cu conductor. A thin **layer** of **passivation dielec**., such as Si nitride, is formed directly over the exposed Cu to **passivate** the Cu. A thin layer of etch stop dielec., such as **Si oxynitride**, is then formed over the **layer** of **passivation dielec**. The **passivation** dielec. is chosen for **passivation** properties and **adhesion** between the **passivation** dielec. and Cu. The etch stop layer is chosen for etch stop properties. The composite layer is thinner than would be required if the **layer** of **passivation dielec**. also provided the etch stop function so that circuit capacitance is reduced by using the composite layer.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:796059 HCAPLUS
DN 132:39063
TI Manufacture of durable silver-aluminum multilayer coating for mirrors with good reflectivity in IR-UV range
IN Wolfe, Jesse D.; Thomas, Norman L.
PA The Regents of the University of California, USA
SO PCT Int. Appl., 27 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9964900	A1	19991216	WO 1999-US12988	19990609

W: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ,
DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS,
JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK,

MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ,
TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD,
RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW, AT, BE, CH, CY, DE, DK,
ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG,
CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

AU 9949555	A1	19991230	AU 1999-49555	19990609
US 6078425	A	20000620	US 1999-329145	19990609

PRAI US 1998-88683P P 19980609
WO 1999-US12988 W 19990609

AB The mirror comprises successively: a substrate comprising .gtoreq.1 reflective layer of Al on its surface, an **adhesion** layer of Ni, Ni nitride, Cr, Cr nitride, Ni-Cr alloys, or Ni-Cr nitride, a 2nd reflective layer of Ag, a **passivation** layer of Ni, Ni nitride, Cr, Cr nitride, Ni-Cr alloys, or Ni-Cr nitride, and .gtoreq.1 durability **layer** of metal **oxides** or metal nitrides. The mirror may further comprises a <25 nm thick amorphous SiO2 layer between the Al and **adhesion** layer. Preferably, the substrate consists essentially of Al; the Al layer is .gtoreq.70 nm thick; the **adhesion** layer is 0.5-10 nm thick; the Ag layer is 10-100 nm thick; the **passivation** layer is 0.5-10 nm thick; the durability layer comprises **Si3N4**, AlN, Si-Al nitride, **Si oxynitride**, SiO2, Al oxynitride, Al2O3, TiO2, Ta-Ha oxide, Ta oxide, Nb2O5, and/or ZrO2. The mirror is manufd. by providing a substrate with the Al layer, and depositing successively the **adhesion** layer, the 2nd reflective layer, the **passivation** layer, and the durability layer. The obtained mirror reflects .gtoreq.90% of all normally incident light in the range of 300-10000 nm.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:664609 HCAPLUS
DN 132:39220
TI Fundamentals of passive oxidation in SiC and **Si3N4**
AU Ogbuji, Linus U. J. T.
CS NASA-Lewis Research Center, Cleveland, OH, 44135, USA
SO Advances in Science and Technology (Faenza, Italy) (1999), 13(Ceramics: Getting into the 2000's, Pt. A), 355-366
CODEN: ASETE5
PB Techna
DT Journal
LA English

AB The very slow oxidn. kinetics of silicon carbide and **silicon nitride**, which derive from their **adherent** and **passivating oxide films**, has been explored at length in a broad series of studies utilizing thermogravimetric anal., electron and optical microg., energy dispersive spectrometry, x-ray diffractometry, micro-anal. depth profiling, etc. Some interesting microstructural phenomena accompanying the process of oxidn. in the two materials will be presented. In **Si3N4** the oxide is stratified, with an SiO2 topscale (which is relatively impervious to O2) underlain by a coherent subscale of **silicon oxynitride** which is even less permeable to O2. Such "defense in depth" endows **Si3N4** with what is perhaps the highest oxidn. resistance of any material, and results in a unique set of oxidn. processes. In SiC the oxidn. reactions are much simpler, yet new issues still emerge; for instance, studies involving controlled devitrification of the amorphous silica scale confirmed that the oxidn. rate of SiC drops by more than an order of

magnitude when the oxide scale fully crystallizes.
RE.CNT 26 THERE ARE 26 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:15756 HCAPLUS
DN 128:109477
TI **Bonding** pad structure and method thereof
IN Ming-tsung, Liu; Hsu, Bill Y. B.; Chung, Hsien-dar; Wu, Der-yuan
PA United Microelectronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5703408	A	19971230	US 1995-419558	19950410
	US 5834365	A	19981110	US 1997-917407	19970825
PRAI	US 1995-419558		19950410		

AB A structure and a process for forming an improved **bonding** pad which allows better **bonding** between a **bond** wire and a metal **bonding** pad. Stripes are formed on a substrate. A conformal **dielec**. **layer**, a conformal barrier layer and a metal layer are formed over the stripes. A **passivation** layer with a window is formed defining a **bonding** pad area. The stripes promote an irregular surface in the barrier and metal layers which reduce stress between the **dielec**. **layer**, the barrier layer and the metal layer. Also, the irregular surfaces increase the barrier metal **adhesion** to the **dielec**. **layer**, reduce **bond** pad peel off, and increase **bonding** yields.

L27 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:504473 HCAPLUS
DN 127:209028
TI Improvement of **adhesion** properties of fluorinated silica glass **films** by nitrous **oxide** plasma treatment
AU Swope, Richard; Yoo, Woo Sik; Hsieh, Julian; Shuchmann, Shari; Nagy, Ferenc; Nijenhuis, Harald Te; Mordo, David
CS Novellus Systems, San Jose, CA, 95134, USA
SO Journal of the Electrochemical Society (1997), 144(7), 2559-2564
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
AB The effects of nitrous oxide plasma surface treatment of fluorinated vitreous silica (FSG) films were investigated to improve film stability and **adhesion** properties. FSG films with varying fluorine concns. were deposited using plasma-enhanced chem. vapor deposition (PECVD), then exposed to a nitrous oxide plasma to modify the surface. Treated films were boiled to study the moisture absorption, and subsequent depositions of foreign **passivation** films such as **silicon nitride**, **silicon oxynitride**, etc., were used to study the changes in **adhesion** characteristics. It was found that plasma treatments under certain conditions could enhance the **adhesion** characteristics of films with higher fluorine dopant levels, but did not measurably change the moisture resistance of the films. The effects of the plasma treatment were confined to the surface and did not measurably effect the bulk properties of the film. The

effects of the nitrous oxide plasma treatment of PECVD FSG films are presented along with proposed mechanisms to explain the effects.

L27 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:704224 HCAPLUS
DN 123:244659
TI Paramagnetic point defects in amorphous thin films of SiO2 and **Si3N4**: updates and additions
AU Poindexter, Edward H.; Warren, William L.
CS Army Res. Lab., Fort Monmouth, NJ, 07703, USA
SO J. Electrochem. Soc. (1995), 142(7), 2508-16
CODEN: JESOAN; ISSN: 0013-4651
DT Journal; General Review
LA English
AB Recent research on point defects in thin films of SiO2, Si nitride, and **Si oxynitride** on Si is presented and reviewed with 55 refs. In SiO2, it now clear that no one type of E' center is the sole source of radiation-induced pos. charge; hydrogenous moieties or other types of E' are proposed. MO theory and easy **passivation** of E' by H2 suggest that release H might depassivate interface Pb sites. A charged E.delta.' center was seen in Cl-free SIMOX (sepn. by implantation of O) and thermal **oxide films**, and it is reassigned to an electron delocalized over four O3.tplbond.Si units around a 5th Si. In **Si3N4**, a new model for the amphoteric charging of .bul.Si.tplbond.N3 moieties is based on local shifts in defect energy with respect to the Fermi level, arising from nonuniform compn.; it does not assume neg. U electron correlation. A new defect NN20 was identified, with dangling orbital on a two-coordinated N atom **bonded** to another N. **Si oxynitride** defects are briefly presented.

L27 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:595310 HCAPLUS
DN 115:195310
TI Effects of oxygen content and **oxide layer** thickness on interface state densities for metal-oxynitride-oxide-silicon devices
AU Xu, Dan; Kapoor, Vik J.
CS Dep. Electr. Comp. Eng., Univ. Cincinnati, Cincinnati, OH, 45221-0030, USA
SO J. Appl. Phys. (1991), 70(3), 1570-4
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The interface state d. of metal-oxynitride-oxide-silicon (MNOS) devices was investigated as a function of the tunnel oxide thickness and the amt. of oxygen in the oxynitride films. Nitrous oxide gas was used to introduce oxygen into the oxynitride film during the deposition process. As 17 at. % oxygen was introduced into the oxynitride **film**, the lowest **oxide**-silicon interface state d. increased from 3.0 to 3.5 .times. 1011 cm-2 eV-1 for 90-.ANG. oxide MNOS devices, and decreased from 5.1 to 3.65 .times. 1011 cm-2 eV-1 for 20 .ANG. oxide devices. The increase in interface state d. with increasing oxygen for 90-.ANG. oxide devices may be due to an increase in the loss of hydrogen **passivation** at the interfacial regions as more oxygen is introduced into the film. The higher interface state d. for the 20 vs 90 .ANG. oxide samples, from the trapping states near or at the oxide-oxynitride interface. However, the decrease in the interface state d. for increasing oxygen concn. for 20-.ANG. oxide MNOS devices may be due to **passivation** of trapping states at the oxide-oxynitride interface by oxygen. The silicon dangling **bonds** responsible for

these trapping states may be compensated by oxygen introduced during the deposition process.

L27 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:582342 HCAPLUS
DN 105:182342
TI Lamination and **adhesion** of thin films
IN Matsuzaki, Kazuo; Saga, Misao
PA Fuji Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61111580	A2	19860529	JP 1984-233452	19841106

AB A method for lamination and **adhesion** of 2 conductive, semiinsulative or **insulative** thin **films** (e.g., Ti and Cu films for bump contacts) on the desired portion of a semiconductor substrate involves formation of a thin film (e.g., Ti-Cu alloy), which is comprised of a compd. from the components of the 2 films, between the 2 films to increase the **adhesion** strength.

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L31  ANSWER 1 OF 14  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:384964  HCAPLUS
DN   136:378483
TI   Dual damascene process for integrated circuits that combines low-K
     dielectric materials and copper
IN   Huang, I-Hsiung; Hwang, Jiunn-Ren; Yen, Yeong-Song; Chang, Ching-Hsu
PA   United Microelectronics Corp., Taiwan
SO   U.S., 9 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE          APPLICATION NO.  DATE
     ---------------   ----  --------      ---------------  --------
PI   US 6391757         B1   20020521      US 2001-875508   20010606
AB   The title dual damascene process involves forming a 1st
     passivation layer, a 1st dielec. layer and a 2nd
     passivation layer on a substrate of a semiconductor wafer.  A 1st
     lithog. and etching process was performed to form at least one via hole in
     the 2nd passivation layer and the 1st dielec. layer.
     Thereafter, a 2nd dielec. layer and a 3rd passivation layer are
     formed on the surface of the semiconductor wafer followed by performing a
     2nd lithog. and etching process to form at least one trench in the 3rd
     passivation layer and the 2nd dielec. layer.  The trench and the
     via hole together construct a dual damascene structure.  Finally, a
     barrier layer and a metal layer are formed on the surface of the
     semiconductor wafer, and a chem.-mech.-polishing (CMP) process was
     performed to complete the dual damascene process.
RE.CNT  12     THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31  ANSWER 2 OF 14  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:51798  HCAPLUS
DN   136:94636
TI   Electronic component and method of manufacture
IN   Henry, Haldane S.; Hill, Darrell G.; Rampley, Colby G.
PA   Motorola, Inc., USA
SO   PCT Int. Appl., 23 pp.
     CODEN: PIXXD2
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE          APPLICATION NO.  DATE
     ---------------   ----  --------      ---------------  --------
PI   WO 2002005347      A2   20020117      WO 2001-US22014  20010711
         W:  AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN,
             CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
             GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR,
             LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT,
             RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ,
             VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
         RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY,
             DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF,
             BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG
     AU 2001082884      A5   20020121      AU 2001-82884    20010711
PRAI US 2000-614794     A    20000712
     WO 2001-US22014    W    20010711
AB   An electronic component includes a substrate and an airbridge located over
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the substrate. The airbridge has at least a 1st layer and a 2nd layer over the 1st layer. The airbridge is elec. conductive where the 1st layer of the airbridge is less resistive than the 2nd layer of the airbridge.

L31 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:23831 HCAPLUS
DN 136:78360
TI Method of more efficiently fabricating a dual damascene structure without residual photoresist problems
IN Huang, I-Hsiung; Hwang, Jiunn-Ren; Hung, Kuei-Chun
PA United Microelectronics Corp., Taiwan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6337269	B1	20020108	US 2001-885042	20010621

AB The present invention fabricates a dual damascene structure. A **passivation** layer, a 1st dielec. layer, a 2nd **passivation** layer, a 2nd dielec. layer, a 3rd **passivation** layer and a 3rd dielec. layer are formed on the surface of the semiconductor wafer followed by etching the 3rd dielec. layer to form a pattern of an upper trench of the dual damascene structure. Then the 3rd **passivation** layer and the 2nd dielec. layer are etched down to the surface of the 2nd **passivation** layer so as to form a pattern of a via hole of the dual damascene structure. Thereafter, the 3rd **passivation** layer and the 2nd **passivation** layer not covered by the 3rd dielec. layer and the 2nd dielec. layer are removed. The 3rd dielec. layer and the 2nd **passivation** layer were used as hard masks to remove the 2nd dielec. layer and the 1st dielec. layer until the surface of the 1st **passivation** layer. Finally, the 2nd **passivation** layer and the 1st **passivation** layer not covered by the 2nd dielec. layer and the 1st dielec. layer are removed to the surface of the conductive layer so completing the process of fabricating the dual damascene structure.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:906181 HCAPLUS
DN 136:30449
TI Multilayer **passivation** process for forming air gaps within a dielectric between interconnections
IN Kim, Jin Yang; Lee, Si-woo; Lee, Won Seoug; Sim, Sang-pil
PA S. Korea
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001051423	A1	20011213	US 1999-432101	19991102
PRAI	KR 1999-5231	A	19990213		

AB A process for forming air gaps within an interlayer dielec. is provided to reduce loading capacitance between interconnections. A 1st dielec. layer is deposited on the spaced interconnections. This 1st dielec. layer is

deposited more thickly at the top sides than at the bottom sides of the interconnections. A 2nd dielec. layer is deposited on the 1st dielec. layer to a controlled thickness that causes formation of air gaps there within between the interconnections. The poor step coverage of the 1st dielec. layer makes it easier to form the air gaps. Air gaps between interconnections allows reduced permittivity of the overall dielec. structures and thereby reduces the interconnect line to line capacitance, and increases the possible operation speed of the semiconductor device.

L31 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:94044 HCAPLUS
DN 134:140453
TI Design and fabrication of chip interconnect wiring structures with low dielectric constant insulators
IN Buchwalter, Leena P.; Callegari, Alessandro Cesare; Cohen, Stephan Alan; Graham, Teresita Ordonez; Hummel, John P.; Jahnes, Christopher V.; Purushothaman, Sampath; Saenger, Katherine Lynn; Shaw, Jane Margaret
PA International Business Machines Corp., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6184121	B1	20010206	US 1998-112919	19980709
PRAI	US 1997-52174P	P	19970710		

AB A method to achieve a very low effective dielec. const. in high performance back end of the line chip interconnect wiring and the resulting multilayer structure are disclosed. The process involves fabricating the multilayer interconnect wiring structure by methods and materials currently known in the state of the art of semiconductor processing; removing the intralevel dielec. between the adjacent metal features by a suitable etching process; applying a thin **passivation** coating over the exposed etched structure; annealing the etched structure to remove plasma damage; laminating an insulating cover layer to the top surface of the **passivated** metal features; optionally depositing an insulating environmental barrier layer on top of the cover layer; etching vias in the environmental barrier layer, cover layer and the thin **passivation** layer for terminal pad contacts; and completing the device by fabricating terminal input/output pads. The method obviates issues such as processability and thermal stability assocd. with low dielec. const. materials by avoiding their use. Since air, which has the lowest dielec. const., is used as the intralevel dielec. the structure created by this method would possess a very low capacitance and hence fast propagation speeds. Such structure is ideally suitable for high d. interconnects required in high performance microelectronic device chips.
RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:736233 HCAPLUS
DN 133:289964
TI Robust copper interconnect structure for VLSI, ULSI, and packages
IN Edelstein, Daniel Charles; Mcgahay, Vincent; Nye, Henry A., III; Ottey, Brian George Reid; Price, William H.
PA International Business Machines Corporation, USA
SO U.S., 5 pp.

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     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.         KIND  DATE            APPLICATION NO.   DATE
     ---------------    ----  --------        ---------------   --------
PI   US 6133136          A    20001017        US 1999-314003    19990519
     WO 2000072380       A1   20001130        WO 2000-GB1847    20000515
         W:  AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR,
             CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU,
             ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU,
             LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE,
             SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW,
             AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
         RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE,
             DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF,
             CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG
     EP 1186034          A1   20020313        EP 2000-931376    20000515
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
PRAI US 1999-314003      A    19990519
     WO 2000-GB1847      W    20000515
AB   A structure comprising a layer of Cu, a barrier layer, a layer of Al-Cu,
     and a pad-limiting layer, wherein the layer of Al-Cu and barrier layer are
     interposed between the layer of Cu and pad-limiting layer.
RE.CNT  7     THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31  ANSWER 7 OF 14  HCAPLUS  COPYRIGHT 2002 ACS
AN   1999:538013  HCAPLUS
DN   131:152692
TI   Solder-bumped semiconductor device having a trench for stress relief
IN   Kleffner, James H.; Mistry, Addi Burjorji
PA   Motorola, Inc., USA
SO   U.S., 5 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.         KIND  DATE            APPLICATION NO.   DATE
     ---------------    ----  --------        ---------------   --------
PI   US 5943597          A    19990824        US 1998-94974     19980615
AB   A bumped semiconductor device including bond pad (12) formed on a
     semiconductor die (10), and a passivation layer (14) overlying
     the semiconductor die and a portion of the bond pad (12).  A solder bump
     (22) is formed so as to overlie the bond pad (12), and a stress isolation
     trench (15) is formed in the passivation layer (14), so as to
     surround the solder bump (22).
RE.CNT  6     THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31  ANSWER 8 OF 14  HCAPLUS  COPYRIGHT 2002 ACS
AN   1999:194400  HCAPLUS
DN   130:204412
TI   Fabrication of multilayered mesa-structured extraction electrode for atom
     probe microanalysis
IN   Lacher, Manfred; Zetterer, Thomas
PA   Institut fuer Mikrotechnik Mainz G.m.b.H., Germany
SO   Ger., 14 pp.
```

CODEN: GWXXAW
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19755990	C1	19990318	DE 1997-19755990	19971217

AB A process for fabrication of an extn. electrode for an atom microprobe was described, in which a first elec. conducting layer is the first electrode and a second elec. conducting layer is the second electrode, each of which is equipped with an aperture of different diam. The electrode is fabricated in several steps using technol. from semiconductor fabrication, which involves (1) deposition of a **passivation** layer on both sides of a thin substrate, (2) deposition of a first and second polymer layer on the first side of the substrate, (3) structuring the second polymer layer by formation of a mesa-structure, (4) deposition of a first elec. conducting layer on the mesa structure, and (5) fabrication of a small aperture in the area of the top of the mesa structure. Following this, addnl. steps are: (1) fabrication of a blind hole on the side of the substrate opposite to the mesa structure through to the first side of the substrate, (2) deposition of a second elec. conducting layer on at least one side of the blind hole on the second side of the substrate, (3) fabrication of an opening in the elec. conducting layer on the second side of the substrate in the area of the mesa structure, and (4) removal of the first and second polymer layers in the area of the mesa structure between the opening in the elec. conducting layer on the first side of the substrate and the opening of the elec. conducting layer on the second side of the substrate.

L31 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:176949 HCAPLUS
DN 130:190570
TI Fabrication of Group IIIA pnictide field effect transistors
IN Shanfield, Stanley R.; Patel, Bharat; Statz, Hermann
PA USA
SO U.S., 8 pp., Cont. of U.S. Ser. No. 825,795, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5880483	A	19990309	US 1993-26222	19930223
PRAI	US 1990-629317		19901218		
	US 1992-825795		19920121		

AB A field effect transistor having a substrate supporting an active layer comprising a Group III-V material. The active layer has a dopant concn. with a source electrode and a drain electrode disposed over and with a gate electrode disposed between the source and drain electrodes in Schottky barrier contact to the active layer. A surface layer portion of the active layer has a neg. charged surface potential disposed between the drain and gate electrodes comprised of said Group III-V material and O. The surface layer portion has a thickness at 25-35 .ANG.. A layer of **passivation** material is disposed at least on the surface layer portion of the active layer.
RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2002 ACS

AN 1998:219317 HCAPLUS
DN 128:277840
TI Double mask hermetic **passivation** method providing enhanced resistance to moisture
IN Bryant, Frank R.; Singh, Abha R.; Cunningham, James A.
PA SGS-Thomson Microelectronics, Inc., USA
SO U.S., 8 pp., Cont.-in-part of U.S. Ser. No. 738,738.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5736433	A	19980407	US 1996-778021	19961231
	JP 10233454	A2	19980902	JP 1997-353242	19971222
PRAI	US 1996-651618		19960522		
	US 1996-738738		19961028		
	US 1996-778021		19961231		

AB A **passivation** structure is formed using two **passivation** layers and a protective overcoat layer using two masking steps. The first **passivation** layer is formed over the wafer and openings are provided to expose portions of the pads for testing the device and fusible links. After testing and laser repair, a second **passivation** layer is formed over the wafer followed a deposit of the protective overcoat. The protective overcoat is patterned and etched, exposing the pads. The remaining portions of the protective overcoat are used as a mask to remove portions of the second **passivation** layer overlying the pads. Leads are then attached to pads and the devices are encapsulated for packaging. The second **passivation** layer overlaps edge portions of the first **passivation** layer at the bond pads to enhance moisture resistance.

L31 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:43067 HCAPLUS
DN 120:43067
TI **Passivation** schemes for copper/polymer thin-film interconnections used in multichip modules
AU Adema, Gretchen M.; Hwang, Lih Tyng; Rinne, A.; Turlik, Iwona
CS Cent. Microelectron., MCNC, Research Triangle Park, NC, 27709, USA
SO IEEE Trans. Compon., Hybrids, Manuf. Technol. (1993), 16(1), 53-9
CODEN: ITTEDR; ISSN: 0148-6411
DT Journal
LA English
AB An investigation was conducted to examine the use of thin inorg. dielec. films as barrier layers between copper and **polyimide**. Emphasis was placed upon discovering the effectiveness of the barrier layers in preventing copper/**polyimide** interaction and detg. its impact on the high frequency elec. performance of transmission line structures. The integrity of the inorg. dielec. layers as diffusion barriers for the copper was analyzed using TEM. These effects were studied by depositing thin layers of **Si3N4**, **SiO2**, and SiOxNy between chromium/copper/chromium lines and either Dow Benzocyclobutene or Dupont 2525 **polyimide**. Both sputtered **Si3N4** and PECVD SiOxNy behaved as diffusion barriers which resulted in improved performance at very high frequencies over unprotected transmission lines. Copper diffused through the sputtered **SiO2** confirming that it is inadequate as a diffusion barrier for copper. Because the thickness of the inorg. dielec. layers was very small in proportion to the thickness of the polymer dielecs. employed, no difference in the effective dielec.

const. was seen over the entire frequency range measured.

L31 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:203317 HCAPLUS
DN 118:203317
TI **Passivation** schemes for copper/polymer thin film interconnections used in multichip modules
AU Adema, Gretchen M.; Hwang, Lih Tyng; Rinne, Glenn A.; Turlik, Iwona
CS MCNC Cent. Microelectron., Research Triangle Park, NC, 27709, USA
SO Proc. - Electron. Compon. Technol. Conf. (1992), 42nd, 776-82
CODEN: PETCES
DT Journal
LA English
AB An investigation was conducted to examine the use of thin inorg. dielec. films as barrier layers between copper and **polyimide**. Emphasis was placed upon discovering the effectiveness of the barrier layers in preventing copper/**polyimide** interaction and detg. its impact on the high frequency elec. performance of transmission line structures. The integrity of the inorg. dielec. layers as diffusion barriers for the copper was analyzed using TEM. These effects were studied by depositing thin layers of **Si3N4**, **SiO2**, and SiOxNy between chromium/copper/chromium lines and either Dow Benzocyclobutene or Dupont 2525 **polyimide**. Both sputtered **Si3N4** and PECVD SiOxNy behaved as diffusion barriers which resulted in improved performance at very high frequencies over unprotected transmission lines. Copper diffused through the sputtered **SiO2** confirming that it is inadequate as a diffusion barrier for copper. Because the thickness of the inorg. dielec. layers was very small in proportion to the thickness of the polymer dielecs. employed, no difference in the effective dielec. const. was seen over the entire frequency range measured.

L31 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:623634 HCAPLUS
DN 111:223634
TI **Passivation** of an integrated circuit
IN Merenda, Pierre; Genot, Bernard
PA SGS-Thomson Microelectronics S. A., Fr.
SO Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 327412	A1	19890809	EP 1989-400042	19890106
	EP 327412	B1	19940921		
	R: DE, GB, IT				
	JP 3054637	B2	20000619	JP 1989-7537	19890113
PRAI	FR 1988-294	A	19880113		

AB In dielec. layer formation for integrated circuit **passivation**, a hard dielec. 1st layer is deposited, followed by spreading out, on the dielec. 1st layer, a viscous dielec. suspension, and annealing to deposit a 2nd hard dielec. layer.

L31 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:588952 HCAPLUS
DN 107:188952
TI Semiconductor device terminal pads
IN Takiar, Hem P.; George, Thomas

PA National Semiconductor Corp., USA
SO Ger. Offen., 5 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 3640249	A1	19870619	DE 1986-3640249	19861125
	JP 62145746	A2	19870629	JP 1986-163500	19860711
PRAI	US 1985-809448		19851216		

AB Semiconductor devices are described in which the terminal pad is formed directly over the active region of the device, the active region being covered and protected by at least a **polyimide** (e.g., PIQ) layer and a through-hole-proof (e.g., Si nitride or **Si oxynitride**) layers. **Passivation** layers (e.g., of **SiO2** or Si-nitride) may underlie the **polyimide** layers. The through-hole-proof layers may be covered by a **passivation** layer. Methods for forming the structures are also described.

L41 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:52458 HCAPLUS
DN 128:174553
TI Surface cleaning and carbonaceous film removal using high pressure, high temperature water, and water/CO2 mixtures
AU **Bakker, Geoffrey L.**; Hess, Dennis W.
CS Dep. Chem. Eng., Lehigh Univ., Bethlehem, PA, 18015, USA
SO Journal of the Electrochemical Society (1998), 145(1), 284-291
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
AB Silicon surface cleaning was investigated using water and water/CO2 mixts. at elevated temp. (100 to 170.degree.C) and elevated pressure [10.3 bar (150 psi) to 137.9 bar (2000 psi)]. Several "model" carbon-contg. materials were invoked to det. the ability of the fluids to remove different forms of carbonaceous layers. Polymethylmethacrylate, amorphous carbon, photoresist (KTI 820), and lab. contamination were studied using XPS to evaluate removal. A model was developed to assist quant. XPS data interpretation by math. simulation of sample surfaces. Results demonstrated that water removed hydrocarbon contamination and polymeric films, but could not remove amorphous carbon layers; water/CO2 mixts. removed all of these materials. Surface cleanliness levels achievable by treating RCA-cleaned silicon and thermally grown silicon dioxide samples with water and water/CO2 were detd. via XPS anal. Native oxide levels and metal contamination resulting from the cleaning cycles were also evaluated.

L41 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:736696 HCAPLUS
DN 126:108042
TI Roles of supports, Pt loading and Pt dispersion in the oxidation of NO to NO2 and of SO2 to SO3
AU Xue, E.; **Seshan, K.**; Ross, J. R. H.
CS Catalysis Group, Faculty of Chemical Technology, University of Twente, Enschede, Neth.
SO Applied Catalysis, B: Environmental (1996), 11(1), 65-79
CODEN: ACBEE3; ISSN: 0926-3373
PB Elsevier
DT Journal
LA English
AB Three types of platinum catalysts, Pt/SiO2, Pt/.gamma.-Al2O3 and Pt/ZrO2 were examd. for the oxidn. of NO to NO2 and of SO2 to SO3. The activity order for both oxidn. reactions was found to be: Pt/SiO2>Pt/.gamma.-Al2O3>Pt/ZrO2. The effect of Pt loading and Pt dispersion on the catalytic activity and selectivity was examd. Over Pt/SiO2, the specific activities were found to be strongly size-dependent, the larger Pt particles exhibiting higher specific activity than the smaller ones. Over the Pt/.gamma.-Al2O3 catalysts, however, the size-dependence appeared to be much less significant than that of the Pt/SiO2 catalysts. The results for Pt/ZrO2 catalysts, however, showed that the specific activities for both reactions were most probably size-independent. The catalytic selectivity for the oxidn. of NO relative to that of SO2 appeared to be size-independent for all the catalysts. The interaction of NO, NO2 and SO2 with the catalysts and the effect of the support on the interaction were investigated using TPD technique. Diesel particle emissions such as soot may be combusted by the NO2.

L41 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:335248 HCAPLUS
DN 125:46193
TI Removal of thermally grown silicon dioxide films using water at elevated temperature and pressure
AU **Bakker, Geoffrey L.**; Hess, Dennis W.
CS Dep. Chem. Eng., Lehigh Univ., Bethlehem, PA, 18015, USA
SO Proceedings - Electrochemical Society (1996), 95-20(Cleaning Technology in Semiconductor Device Manufacturing), 464-471
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB The removal of thermally grown silicon dioxide films from silicon wafer surfaces with water at elevated temp. and pressure was studied using ellipsometry and XPS. Complete removal of 50-nm silicon dioxide layers was obsd. with XPS after exposure of the sample to de-ionized (18 M-ohm-cm) water at 280.degree. and 241 bar (3500 psi) for 30 min. To the detection limit of XPS (.apprx.0.5 at.%), no metal contamination was deposited on the surface. Removal rates were detd. at temps. between 260 and 305.degree. at 138 bar (2000 psi). A surface reaction limited rate equation, used previously to describe quartz dissoln. in water over a wide range of temp., was used to est. rate consts. for silicon dioxide removal. An effective activation energy of 76.7 kJ/mol was calcd. for the etching process, which is comparable to values reported for quartz dissoln. under similar conditions (62.6-79.0 kJ/mol).

L41 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:930635 HCAPLUS
DN 123:323293
TI Removal of thermally grown silicon dioxide films using water at elevated temperature and pressure
AU **Bakker, Geoffrey L.**; Hess, Dennis W.
CS Dep. Chem. Eng., Lehigh Univ., Bethleham, PA, 18015, USA
SO J. Electrochem. Soc. (1995), 142(11), 3940-4
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB The removal of thermally grown silicon dioxide films from silicon wafer surfaces with water at elevated temp. and pressure was studied using ellipsometry and XPS. Complete removal of 50 nm silicon dioxide layers was obsd. with XPS after exposure of the sample to deionized (18 M.OMEGA. cm) water at 280.degree. and 241 bar (3500 psi) for 30 min. To the detection limit of XPS (.apprx.0.5 at. percent), no metal contamination was deposited on the surface. Removal rates were detd. at temps. between 260 and 305.degree. at 138 bar (2000 psi), and increased from 2.9 to 11.2 nm/min over this temp. range. A surface reaction limited rate equation, used previously to describe quartz dissoln. in water over a wide range of temp., was used to est. rate consts. for silicon dioxide removal. Calcd. rate consts. were higher than reported values for quartz dissoln., presumably due to the amorphous structure of thermally grown silicon dioxide. An activation energy of 76.6 kJ/mol was calcd. for the etching process, which is comparable to values reported for quartz dissoln. under similar conditions (62.6-79.0 kJ/mol). The agreement of activation energy values indicates that the dissoln. mechanism may be similar for thermal silicon dioxide and quartz. Surface roughening was examd. for silicon and silicon dioxide samples via at. force microscopy and SEM. Silicon dioxide surfaces showed low surface roughening, while silicon samples had significant amts. of silicon dioxide redeposited on the surface.

Microbalance measurements indicated that silicon surfaces etched .apprx.25 times faster than thermally grown silicon dioxide, accounting for the silicon dioxide redeposition.

L41 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:100099 HCAPLUS
DN 102:100099
TI The nature and source of copper smelter particulate emissions
AU Whyte, John R., Jr.; Geiger, Gordon H.; **Seshan, Krishna**
CS R and D Cent., Freeport Min. Corp., Belle Chasse, LA, 70037, USA
SO Metall. Trans. B (1984), 15(4), 617-22
CODEN: MTTBCR; ISSN: 0360-2141
DT Journal
LA English
AB Particles from the inlet, outlet, and bin of electrostatic precipitators operating on Cu reverberatory furnace and converter off-gas streams were characterized by their chem., mineralog., morphol., and elec. properties. Reverberatory furnace particles, nominally <10 .mu. in size, are formed by condensation of PbSO4 and ZnSO4 onto oxide particles (Fe3O4, Cu2O, SiO2) originating in the slag or conc. The very fine particles from the dual-nature converter dust were similar in characteristics and probably in origin to the reverberatory furnace particles. The coarse (.ltoreq.500 .mu.) slag (Fe3O4, SiO2) and matte (Cu2S, Cu) particles in the converter samples probably arose from entrainment by flowing or bubbling gases. The properties of all 3 sample portions varied depending on the source of the sample and the effectiveness of electrostatic pptn.

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File    2:INSPEC  1969-2002/Aug W2
        (c) 2002 Institution of Electrical Engineers
*File    2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.

Set      Items   Description
S1       44053   (SILICON OR SI)()(DIOXIDE OR O2) OR SILICA## OR SILICATE OR
                  KEATITE OR HYALITE OR LECHATELIERITE OR QUARTZ OR SIDERITE OR
                  SIFRACO OR CHALCEDONY OR QUARTZINE OR CRISTOBALITE OR COESITE
                  OR STISHOVITE OR CHRYSOPRASE OR SIO2
S2         938   (SILICON OR SI)()(OXYNITRIDE) OR DISILICON OXYNITRIDE OR S-
                 ILICON OXIDE(N)NITRIDE OR SI2ON2
S3        8816   (SILICON OR SI3)()(NITRIDE OR N4) OR SI3N4 OR BAYSINID OR -
                 DENKA OR ROYDAZIDE OR NIERITE
S4       36504   (INSULAT? OR OXIDE OR DIELECTRIC)(2N)(LAYER? OR FILM OR CO-
                 AT????)
S5      312829   ADHESI? OR ADHERE? OR STICK? OR CLING? OR BOND? OR CEMENT?
                 OR CONGLUTIN? OR AGGLUTIN? OR MUCILAG? OR TACK? OR GLUE? OR G-
                 LUING? ? OR PASTE? OR PASTING? ? OR GUM? OR HOLD? OR GRIP? OR
                 GRASP? OR BIND?
S6        6995   CI=(SI SS(S) O SS)(S) NE=2
S7        2178   CI=(SI SS(S) O SS(S) N SS)(S) NE=3
S8        2864   CI=(SI SS(S) N SS)(S) NE=2
S9        1607   S4 AND (S6 OR S1)
S10        375   S5 AND (S7 OR S2)
S11        650   PASSIVAT? AND (S3 OR S8)
S12     304660   IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MI-
                 CRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR M-
                 ICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR
                  MICROELECTRONIC? OR CC=B2220
S13        422   S12 AND S9
S14          7   S13 AND S11
S15          3   S13 AND S10
S16         10   S14 OR S15
S17         11   S13 AND POLYIMIDE? ?
S18         11   S17 NOT (S14 OR S15)
S19       2718   S12 AND PASSIVAT?
S20        164   S19 AND POLYIMIDE? ?
S21          1   S20 AND S9
S22          0   S20 AND S10
S23         20   S20 AND (S3 OR S8)
S24         20   S23 NOT (S14 OR S15 OR S17)
```

16/3,AB/1
DIALOG(R)File 2:INSPEC

6954235 INSPEC Abstract Number: A2001-14-6630Q-001, B2001-07-2550F-036
Title: Effects of dielectric materials on electromigration failure
Author(s): Doan, J.C.; Lee, S.; Lee, S.-H.; Flinn, P.A.; Bravman, J.C.; Marieb, T.N.
Author Affiliation: Dept. of Mater. Sci. & Eng., Stanford Univ., CA, USA
Journal: Journal of Applied Physics vol.89, no.12 p.7797-808
Publisher: AIP,
Publication Date: 15 June 2001 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(20010615)89:12L.7797:EDME;1-Q
Material Identity Number: J004-2001-011
U.S. Copyright Clearance Center Code: 0021-8979/2001/89(12)/7797(12)/$18.00
Language: English
Abstract: The effects of **dielectric layers** on electromigration failure were studied in situ using a high-voltage scanning electron microscope and at the **wafer** level using conventional accelerated testing. Several different **passivation** layers were deposited on **wafers** with Al interconnect test structures. Prior to the deposition of the final dielectric, the **wafers** were processed identically and, whenever possible, simultaneously. Interconnects encapsulated with compliant polymer and very thin (0.1 mu m) SiO/sub 2/ layers demonstrated substantial lifetime extensions over those with more rigid (1 mu m thick) SiO/sub 2/ layers. Unpassivated lines behaved dramatically differently and failed much sooner than those covered with only 0.1 mu m of SiO/sub 2/. As expected, increasing the **passivation** thickness from 0.5 to 4 mu m increased the electromigration lifetime for SiO/sub 2/ covered specimens. The fabrication of **silicon dioxide** dielectrics using electron-cyclotron-resonance chemical-vapor deposition (CVD) and **silicon nitride** dielectrics via plasma-enhanced CVD damaged the interconnects. This damage nearly completely removed the barrier to void nucleation during electromigration.
Subfile: A B

16/3,AB/2
DIALOG(R)File 2:INSPEC

6209591 INSPEC Abstract Number: B1999-05-2550F-026
Title: Microstructure evolution of Al-1.5%Cu alloy as a function of resistance change due to isothermal DC stressing
Author(s): Lee, T.; Schade, M.; Merino, A.; Lee, J.; Christenson, C.; Varker, C.; Evans, K.
Author Affiliation: Motorola Inc., Phoenix, AZ, USA
Conference Title: Materials Reliability in Microelectronics VIII. Symposium p.109-14
Editor(s): Bravman, J.C.; Marieb, T.N.; Lloyd, J.R.; Korhonen, M.A.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1998 Country of Publication: USA xi+365 pp.
ISBN: 1 55899 422 X Material Identity Number: XX-1999-00051
Conference Title: Materials Reliability in Microelectronics VIII. Symposium

Conference Date: 13-16 April 1998 Conference Location: San Francisco, CA, USA
Language: English
Abstract: This paper investigates Cu segregation and void morphology along AlCu alloy metal lines as a function of resistance change resulting from isothermal DC stressing at 225 degrees C and a current density J=2*10/sup 6/ A/cm/sup 2/. The Al-1.5wt.%Cu alloy was deposited via DC magnetron sputtering on a Si substrate at 525 degrees C with a 1500 AA TiW barrier layer. NIST test structures (length of 800 mu m, thickness of 1.2 mu m, widths of 5 and 10 mu m) were utilized in this study. BPSG was used as the **insulation layer** between the Si substrate and conductor. The surface **passivation** layer was composed of Si/sub 3/N/sub 4/-PSG. Various failure criteria were selected to explore the correlation between Cu segregation and void morphology along the metal line and the relative percentage resistance change (Delta R/R). The log-normal plots, mean times-to-failure, and sigmas at each Delta R/R (-2%, 2%, 5%, 10%, 20%, 100%, 250%) were plotted and listed. The microstructural evolution in terms of void morphology was monitored using SEM. SEM-EDS was used to analyze the Cu concentrations along metal lines tested at various % Delta R criteria.
Subfile: B

16/3,AB/3
DIALOG(R)File 2:INSPEC

6189510 INSPEC Abstract Number: B1999-04-2570F-007
Title: Alternative gate dielectrics with BST/TiO/sub 2//(barrier oxide) stacked structure
Author(s): Jeon, Y.; Lee, B.H.; Zawadzki, K.; Qi, W.-J.; Lee, J.C.
Author Affiliation: Microelectron. Res. Center, Texas Univ., Austin, TX, USA
Conference Title: Rapid Thermal and Integrated Processing VII. Symposium p.193-8
Editor(s): Ozturk, M.C.; Roozeboom, F.; Timans, P.J.; Pas, S.H.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1998 Country of Publication: USA xiii+403 pp.
ISBN: 1 55899 431 0 Material Identity Number: XX-1998-03125
Conference Title: Rapid Thermal and Integrated Processing VII. Symposium
Conference Date: 13-15 April 1998 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The BaSrTiO/sub 3/ (BST)/TiO/sub 2//(barrier **layer**) stacked **dielectric** structure has been proposed for ultra thin (<20 AA) gate dielectric applications to overcome the direct tunneling current problem of SiO/sub 2/. To characterize the alternative dielectrics, MIM and MIS capacitors were fabricated. TiO/sub 2/ is believed to prevent BST and Si from reaction and interdiffusion while TiO/sub 2/-Si itself is stable due to the strong **binding** energy. For better TiO/sub 2/-Si interfacial quality, a proper barrier layer is needed between TiO/sub 2/ and Si. Optimization of this barrier layer was performed using RTP grown N/sub 2/O oxide and self-grown interfacial **oxide layers** with various annealing conditions. To monitor these barrier layers, TEM and electrical analysis were performed. From TEM observation, it was found that the interfacial layer was formed in every sample whether it was intentionally grown or not. It was observed that the leakage current of Pt-TiO/sub 2/-Si dramatically increased after 700 degrees C or higher temperature annealing. This may be related to the TiO/sub 2/ crystal

structure transition from anatese to rutile at about 700 degrees C (Spitzer et al, 1991). It was also found that both Pt-BST-TiO/sub 2/-Si and Pt-TiO/sub 2/-Si showed lower leakage current compared to the conventional NO oxide at comparable equivalent SiO/sub 2/ thickness. These results imply that these materials **hold** some promise as alternatives to pure SiO/sub 2/ in the very thin range.
Subfile: B

16/3,AB/4
DIALOG(R)File 2:INSPEC

5727561 INSPEC Abstract Number: B9712-2550F-011
Title: Electromigration in aluminum/silicon/copper metallization due to the presence of a thin **oxide layer**
Author(s): Koh, K.A.; Chua, S.J.
Author Affiliation: Brooktree Pte, Kolam Ayer Ind. Park, Singapore
Journal: Journal of Electronic Materials Conference Title: J. Electron. Mater. (USA) vol.26, no.9 p.1070-5
Publisher: TMS,
Publication Date: Sept. 1997 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(199709)26:9L.1070:EASC;1-K
Material Identity Number: J246-97010
U.S. Copyright Clearance Center Code: 0361-5235/97/$5.00
Conference Title: Evolution and Advanced Characterization of Thin Film Microstructures. TMS 1997 Annual Meeting
Conference Date: 9-13 Feb. 1997 Conference Location: Orlando, FL, USA
Language: English
Abstract: The effect of a thin layer of SiO/sub 2/ (50 nm) on the electromigration behavior of Al/0.8wt.%Si/0.5wt.%Cu metallization, **passivated** by spin-on-glass, phosphorus **silicate** glass and **silicon nitride** as part of the complementary metal oxide semiconductor technology fabrication process was studied. It is found that voids were formed along the edge of the metallization line as opposed to formation at triple point of grain boundaries. At the same stress current of 1*10/sup 6/ A/cm/sup 2/, thicker metallization layer (600 nm) showed an improvement in median time to failure (MTF) (1.4 times) with smaller void size (0.2 to 0.4 mu m) over one without an underlying oxide, whereas if the metallization thickness is thin (300 nm), the MTF is degraded (0.6 times) with larger void size formed (0.3 to 1.0 mu m).
Subfile: B

16/3,AB/5
DIALOG(R)File 2:INSPEC

5533246 INSPEC Abstract Number: A9709-7340Q-010, B9705-2530F-021
Title: Low-dose SIMOX approach and stimulating factors
Author(s): Litovchenko, V.; Romanyuk, B.; Efremov, A.; Klyui, M.; Mel'nik, V.P.
Author Affiliation: Inst. of Semicond. Phys., Acad. of Sci., Kiev, Ukraine
Conference Title: Proceedings of the Seventh International Symposium on Silicon-On-Insulator Technology and Devices p.117-20

Editor(s): Hemment, P.L.F.; Cristoloveanu, S.; Izumi, K.; Houston, T.; Wilson, S.
Publisher: Electochem. Soc, Pennington, NJ, USA
Publication Date: 1996 Country of Publication: USA ix+440 pp.
Material Identity Number: XX96-02880
Conference Title: Proceedings of Seventh International Symposium on Silicon-on- Insulator Technology and Devices
Conference Date: 5-10 May 1996 Conference Location: Los Angeles, CA, USA
Language: English

Abstract: The conventional SIMOX method for creation of SOI structures in Si needs either very high doses of implanted oxygen together with very high annealing temperatures, or lower implantation doses using multistage implantation-annealing procedures. Recently, a new set approaches were proposed to improve this technology and achieve a thin buried **oxide layer**. In particular, high-dose Ar/sup +/ preimplantation or combined (O/sup +/+N/sup +/) implantation were used, mostly in order to compensate for mechanical stress induced by the difference between Si-Si and Si-O chemical **bonds** length. In previous presentations, we have also proposed a combined (O/sup +//sub 2/+C/sup +/) implantation. In this case, the carbon dissolved in the Si matrix plays a triple role: firstly as a compensator for atomic volume misfit and thus for the macroscopic strain and stress induced after SiO/sub 2/ precipitation, secondly as a source of excess vacancies (or vacancy clusters), and finally as a getter which attracts oxygen and in such a manner facilitates the SiO/sub 2/ phase creation.

Subfile: A B

16/3,AB/6
DIALOG(R)File 2:INSPEC

5412834 INSPEC Abstract Number: A9624-7830-002
Title: Raman scattering studies on interface stresses in AlN and SiO/sub x/N/sub y/ films on GaAs substrates
Author(s): Hou Yongtian; Zhang Shulin; Gao Yuzhi; Yin Hongkun; Ning Baojun; Li Ting; Zhang Lichun
Author Affiliation: Dept. of Phys., Beijing Univ., China
Journal: Chinese Journal of Semiconductors vol.15, no.12 p.809-13
Publisher: Chinese Journal Semicond,
Publication Date: Dec. 1994 Country of Publication: China
CODEN: PTTPDZ ISSN: 0253-4177
SICI: 0253-4177(199412)15:12L.809:RSSI;1-A
Material Identity Number: A658-96003
Language: Chinese

Abstract: The interface stresses in AlN and SiO/sub x/N/sub y/ films on GaAs **wafers** have been studied with Raman spectroscopy technique. The effect of heat treatment in N/sub 2/ and Ar atmosphere on the interface stress is also examined. The results show that, contrary to deposited SiO/sub x/N/sub y/ film, the AlN film sputtered on GaAs **wafers** has much less interface stress and remains stable for annealing both in N/sub 2/ and Ar atmosphere. All these demonstrate that AlN film is a suitable **passivation** or **insulating film** for GaAs device technology.

Subfile: A

16/3,AB/7
DIALOG(R)File 2:INSPEC

5233579 INSPEC Abstract Number: B9605-2570D-042
Title: The role of SOG and oxynitride **passivation** in the field inversion of CMOS circuits
Author(s): Ghneim, S.; Fulford, J.
Author Affiliation: Adv. Micro Devices Inc., Austin, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2635 p.130-5
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1995 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1995)2635L.130:ROPF;1-0
Material Identity Number: C574-95262
U.S. Copyright Clearance Center Code: 0 8194 2001 8/95/$6.00
Conference Title: Microelectronic Manufacturing Yield, Reliability, and Failure Analysis
Conference Sponsor: SPIE
Conference Date: 25-26 Oct. 1995 Conference Location: Austin, TX, USA
Language: English
Abstract: N-channel field inversion leakage in multilevel-metal CMOS processes is one of the adverse effects of back-end-of-line (BEOL) processing. In particular, using certain combinations of nitride **passivation** films, spin-on-glass (SOG), and TEOS planarization was shown to be very detrimental to the stability of CMOS circuits because of the induced leakage under field oxides. This work reports on a new field inversion leakage that is totally due to silicon oxynitride **passivation**. The SOG film used to planarize the intermetal **dielectric** (IMD) **layers** did not have a significant role in the field inversion leakage as we were able to induce and suppress leakage currents by only controlling the oxynitride **passivation** deposition conditions (with and without the SOG). In particular, it is shown that a high oxynitride deposition temperature induces severe parasitic leakage currents while a low deposition temperature diminishes the leakage.
Subfile: B
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16/3,AB/8
DIALOG(R)File 2:INSPEC

4621546 INSPEC Abstract Number: A9408-6860-011
Title: Electron-beam-induced nitrogen migration through a nitrided **silicon dioxide** thin film
Author(s): Garcia, V.; Glachant, A.; Pantel, R.; Straboni, A.
Author Affiliation: Centre de Recherche sur les Mecanismes, Marseille Univ., Luminy, France
Journal: Applied Surface Science vol.74, no.2 p.165-70
Publication Date: Feb. 1994 Country of Publication: Netherlands
CODEN: ASUSEE ISSN: 0169-4332
U.S. Copyright Clearance Center Code: 0169-4332/94/$07.00
Language: English
Abstract: Auger sputter depth profiles of very thin (15 nm) plasma-nitrided SiO/sub 2/ films thermally grown on silicon **wafers**

have been measured before and after bombardment with energetic electrons (1, 3, or 5 keV). Electron irradiation of the film induced nitrogen depletion at the vacuum/dielectric interface and a nitrogen pile-up at the dielectric/silicon interface. Our results indicate that this phenomenon is maximum for the lowest primary electron energy. This behavior could be understood on the basis of an electron-stimulated Si-N **bond** decomposition and the creation of positive nitrogen ions. The released nitrogen ions could either escape into the vacuum or migrate through the **dielectric layer** and pile up at the dielectric/silicon interface due to the existence inside the layer of a non-uniform electric field, in agreement with recent theoretical predictions.
Subfile: A

16/3,AB/9
DIALOG(R)File 2:INSPEC

01749103 INSPEC Abstract Number: A81087385, B81046077
Title: Plasma deposition of **silicon dioxide** and **silicon nitride** films
Author(s): van de Ven, E.P.G.T.
Author Affiliation: Philips Res. Labs., Sunnyvale, CA, USA
Journal: Solid State Technology vol.24, no.4 p.167-71
Publication Date: April 1981 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
Language: English
Abstract: Plasma deposition processes for **silicon dioxide** and **silicon nitride** are compared and the various applications discussed. The optimization of both processes requires a different approach which is determined primarily by the nature of the reaction gases used. For plasma oxide, control of the gas phase reactions has to be maintained to prevent particles, pinholes and other localized structural defects, whereas for plasma nitride the surface reactions are critical. The applications for which the films are used are determined by their effect on the device electrical parameters. Both plasma oxide and nitride are successfully used for device **passivation** and interlayer insulation; in addition, plasma oxide can also be used as an **insulating layer** in high voltage **ICs** and devices with critical dopant profiles.
Subfile: A B

16/3,AB/10
DIALOG(R)File 2:INSPEC

00078527 INSPEC Abstract Number: B70000456
Title: Thin **film dielectric** materials for **microelectronics**
Author(s): Zaininger, K.H.; Wang, C.
Journal: Proceedings of the IEEE vol.57, no.9 p.1564-70
Publication Date: Sept. 1969 Country of Publication: USA
CODEN: IEEPAD ISSN: 0018-9219
Language: English
Abstract: Important applications of dielectric films used in modern **integrated circuit** technology include dielectric insulation, surface **passivation** , diffusion masking, radiation resistance, and hermetic seal. These many functional applications pose stringent requirements on the various properties of the insulating films and the

methods used for their preparation. To data **silicon dioxide** (SiO_2) has been used almost exclusively because of (1) its ease of preparation, (2) its well-understood properties, and (3) its generally good compatibility and satisfactory interface with silicon. There are, however, drawbacks to the use of SiO_2 and other materials have been sought for better performance, greater versatility, higher reliability, and lower cost. These include binary metal oxides and **silicon nitride**.
The state of the art of thin **film dielectric** materials for **microelectronics** is reviewed in this paper. The role of thin film dielectrics for devices is presented, and new and known materials are discussed for potential applications.

18/3,AB/1
DIALOG(R)File 2:INSPEC

7288789 INSPEC Abstract Number: B2002-07-2575F-026
Title: Micromachined **chips** for biomolecular investigation
Author(s): Ilie, M.; Cianci, E.; Foglietti, V.; de Bellis, G.; Caramenti, G.
Author Affiliation: CNR-IESS, Roma, Italy
Conference Title: Proceedings of the euspen. 2nd International Conference Part vol.1 p.16-19 vol.1
Editor(s): Balsamo, A.; Evans, C.; Frank, A.; Knapp, W.; Mana, G.; Mortarino, M.; Sartori, S.; Thwaite, E.G.
Publisher: euspen, Cranfield Univ, Bedford, UK
Publication Date: 2001 Country of Publication: UK 2 vol. xxvii+855 pp.
Material Identity Number: XX-2001-01634
Conference Title: Proceedings of 2001 euspen's 2nd International Conference
Conference Date: 27-31 May 2001 Conference Location: Turin, Italy
Language: English
Abstract: The realisation of a matrix of separately driven electrodes, dedicated to biological analysis, is described. Silicon anisotropic etching and **polyimide** patterning are used for obtaining the analysis, inlet and outlet analyte reservoirs. Techniques as oxidation, metal evaporation, PE-CVD deposition and RIE have been used, as well as the e-beam direct writing, in order to pattern the matrix of gold electrodes. The **insulating layers** were thermally grown **silicon dioxide** and PECVD silicon nitride. Optical and SEM microscopy has been used for dimensional characterisation of the **chip** as well as electric measurements of the electrodes connections. Fluorescent DNA molecules driving experiment has been performed after mounting the device in dedicated LIF detection set-up.
Subfile: B

18/3,AB/2
DIALOG(R)File 2:INSPEC

6050655 INSPEC Abstract Number: A9822-7920H-001, B9811-2320-018
Title: Determination of secondary electron yield from insulators due to a low-kV electron beam
Author(s): Yong, Y.C.; Thong, J.T.L.; Phang, J.C.H.
Author Affiliation: Dept. of Electr. Eng., Nat. Univ. of Singapore, Singapore
Journal: Journal of Applied Physics vol.84, no.8 p.4543-8
Publisher: AIP,
Publication Date: 15 Oct. 1998 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19981015)84:8L.4543:DSEY;1-D
Material Identity Number: J004-98019
U.S. Copyright Clearance Center Code: 0021-8979/98/84(8)/4543(6)/$15.00
Language: English
Abstract: A technique for the accurate determination of secondary electron (SE) yield of insulators due to low-kV electron beam is presented. It is based on a capacitatively coupled charge measurement by subjecting

the **insulating film** to a controlled pulsed electron beam in a scanning electron microscope. SE emissions from several insulating materials employed in **integrated circuit** manufacturing including wet and sputtered **silicon dioxide** (SiO/sub 2/), **polyimide** , and AZ1350J photoresist, have been investigated for a range of primary energies between 0.5 and 2.5 keV. Comparisons are made between experimental data for SiO/sub 2/ and **polyimide** with previous results. The dependence of SE emission on incidence angle and topography for SiO/sub 2/ was investigated. Experimental results indicate that the dependence of SE emission on surface tilt for SiO/sub 2/ is in good agreement with the power law for tilt angles below 70 degrees , while emission saturation is observed at higher tilt angles. The SE yield from sputtered oxide was found to be higher than that of wet oxide, which is related to differences in topography between the two materials.
Subfile: A B

18/3,AB/3
DIALOG(R)File 2:INSPEC

04383140 INSPEC Abstract Number: A9310-8115L-006, B9305-0520-008
Title: A fast laser alloying process for the selective electroplating of metal on SiO/sub 2/ and **polyimide**
Author(s): Malba, V.; Bernhardt, A.F.
Author Affiliation: Lawrence Livermore Nat. Lab., CA, USA
Conference Title: Photons and Low Energy Particles in Surface Processing Symposium p.91-6
Editor(s): Ashby, C.I.H.; Brannon, J.H.; Pang, S.W.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1992 Country of Publication: USA xv+552 pp.
Conference Date: 3-6 Dec. 1991 Conference Location: Boston, MA, USA
Language: English
Abstract: A new laser direct-write process for patterning of metal on multichip modules has been developed. The process involves the laser modification of the nonconductive surface of a seed multilayer, converting it to a conductive surface, which can be electroplated with metal. The seed multilayer is composed of a TiW adhesion layer, onto which a Au film is sputtered, followed by an a-Si layer, which forms the nonconductive surface. The laser modifies the surface by alloying (or mixing) the Si and Au to form the conductive surface. This laser process has been shown to be capable of writing speeds of 2.5 m/s. With a **silicon dioxide** interlevel **dielectric layer** , the process works over a large range of laser power (P/sub max//P/sub min/ approximately 5). A **polyimide** interlevel **dielectric layer** can be used without damage or loss of adhesion, although the process margin is substantially reduced (P/sub max//P/sub min/ approximately 2).
Subfile: A B

18/3,AB/4
DIALOG(R)File 2:INSPEC

04106049 INSPEC Abstract Number: B9204-2550F-022
Title: Thin film interconnect processes
Author(s): Malik, F.
Author Affiliation: Intel Corp., Rio Rancho, NM, USA

Journal: Thin Solid Films vol.206, no.1-2 p.70-5
Publication Date: 10 Dec. 1991 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
U.S. Copyright Clearance Center Code: 0040-6090/91/$3.50
Conference Title: 18th International Conference on Metallurgical Coatings and Thin Films
Conference Date: 22-26 April 1991 Conference Location: San Diego, CA, USA
Language: English
Abstract: Interconnects and associated photolithography and etching processes play a dominant role in the feature shrinkage of electronic devices. Most interconnects are fabricated by use of thin film processing techniques. Planarization of dielectrics and novel metal deposition methods are the focus of current investigations. Spin-on glass, **polyimides**, etch-back, bias-sputtered **quartz** and plasma-enhanced conformal films are being used to obtain planarized dielectrics over which metal films can be reliably deposited. Recent trends have been towards chemical vapor depositions of metals and refractory metal silicides. Interconnects of the future will be used in conjunction with planarized **dielectric layers** . Reliability of devices will depend to a large extent on the quality of the interconnects.
Subfile: B

18/3,AB/5
DIALOG(R)File 2:INSPEC

03057743 INSPEC Abstract Number: B88007675
Title: **Polyimides** (VLSI application)
Author(s): Lee, Y.K.; Fryd, M.
Author Affiliation: Marshall Res. & Dev. Lab., E.I. du Pont de Nemours & Co., Philadelphia, PA, USA
Book Title: Chemistry of the semiconductor industry p.282-91
Editor(s): Moss, S.J.; Ledwith, A.
Publisher: Blackie, Glasgow, UK
Publication Date: 1987 Country of Publication: UK xiv+426 pp.
ISBN: 0 216 92005 1
Language: English
Abstract: The movement in the semiconductor industry towards VLSI leads to multilayer construction and feature sizes of 1 mu m or less. This development requires that the interlevel **dielectric layer** be able to planarize the underlying topography sufficiently to provide good step coverage for the next layer of metal. One solution is the use of **polyimides** which have the following advantages over good thermal, mechanical and electrical properties; commercial availability of high-purity materials of various grades; ability to be processed by standard photolithographic and various dry etching schemes; and good adhesion to **silicon dioxide** substrate (after priming), aluminium alloys and themselves.
Subfile: B

18/3,AB/6
DIALOG(R)File 2:INSPEC

02790902 INSPEC Abstract Number: B87001438
Title: The performance and processing of a new spin-on polysiloxane

interlevel dielectric material
Author(s): Whitwell, G.E.; Wade, T.E.
Author Affiliation: Stauffer Chem. Co., Dobbs Ferry, NY, USA
Conference Title: 1986 Proceedings Third International IEEE VLSI Multilevel Interconnection Conference (Cat. No. 86CH2337-4) p.292-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 536 pp.
U.S. Copyright Clearance Center Code: CH2337-4/86/0000-0292$01.00
Conference Sponsor: IEEE
Conference Date: 9-10 June 1986 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: The performance of a spin-on interlevel dielectric material which is composed of curable polysiloxanes in an organic carrier is described. It provides an **insulating** and passivating **layer** which can separate device features and/or conduction path levels of an **integrated circuit** . The material displays excellent thermal stability, low water absorption and good adhesion to **silicon dioxide** and aluminum. Resistance and dielectric property measurements give values similar to those reported for **polyimides**. C-V plots show low mobile ion content. Films of 1- mu m thickness are easily spun onto **wafers** and the thickness can be varied by both spin speed and solids content. Reasonable planarization is achieved, and the material may be plasma etched. The formulation, which is neither pure inorganic nor pure organic, offers many of the advantages of each and meets or exceeds the specifications of currently used materials.
Subfile: B

18/3,AB/7
DIALOG(R)File 2:INSPEC

02790879 INSPEC Abstract Number: B87001788
Title: A novel multilevel metallization technique for advanced CMOS and bipolar **integrated circuits**
Author(s): Grewal, V.; Gschwandtner, A.; Higelin, G.
Author Affiliation: Siemens AG, Munich, West Germany
Conference Title: 1986 Proceedings Third International IEEE VLSI Multilevel Interconnection Conference (Cat. No. 86CH2337-4) p.107-13
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 536 pp.
U.S. Copyright Clearance Center Code: CH2337-4/86/0000-0107$01.00
Conference Sponsor: IEEE
Conference Date: 9-10 June 1986 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: A CMOS-compatible technique for multilevel metallization is described that is based on an etch-back process in which LPCVD-SiO/sub 2/ is the main **dielectric layer**, but cavities with extreme aspect ratio (one or more) are filled with **polyimide**. The same **polyimide** , with a low degree of planarization (20-40%), is used as the sacrificial layer for the etch-back process. The emphasis in this technique is to replicate, in the intermetal dielectric, the basic topography of the flowed borophosphosilicate glass below the first-level metallization. Deposition of SiO/sub 2/ after the etch-back process results in a fairly smooth surface with relatively uniform oxide thickness over the metal conductors, independent of the underlying topography. This facilitates the etching of properly shaped vias and good step coverage of

subsequent metallization. The technique was tested on CMOS memory **integrated circuits** with 1.2- mu m design rules.
Subfile: B

18/3,AB/8
DIALOG(R)File 2:INSPEC

01749211 INSPEC Abstract Number: B81046198
Title: Composite insulators (for **integrated circuits**)
Author(s): Bartush, T.A.; Brooks, G.A.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.23, no.11 p.4907
Publication Date: April 1981 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: Dual **dielectric layers** are provided for **integrated circuits** by a process which does not increase the number of resist masking levels. The first level metal pattern is defined followed by the formation of interconnecting metal studs by any suitable procedure. A thin blanket layer of silicon nitride is deposited at low temperature from a plasma, followed by a **quartz** layer such that the **quartz** surface is at the same height as the studs. The surface is then planarized by coating it with a layer of resist or **polyimide**. The structure is then dry etched in a plasma which removes **quartz** and resist or **polyimide** at about the same rate, with the etching continued until the nitride is removed from the top of the studs. The second level metal pattern is then formed by standard processing.
Subfile: B

18/3,AB/9
DIALOG(R)File 2:INSPEC

01729971 INSPEC Abstract Number: B81040524
Title: Multilevel metal interconnect for VLSI circuits using polyamide dielectrics
Author(s): Wade, T.E.
Author Affiliation: Dept. of Electrical Engng., Mississippi State Univ., Mississippi State, MS, USA
Conference Title: IEEE SOUTHEASTCON 1981 Conference Proceedings p. 12-16
Publisher: IEEE, New York, NY, USA
Publication Date: 1981 Country of Publication: USA 913 pp.
Conference Sponsor: IEEE
Conference Date: 5-8 April 1981 Conference Location: Huntsville, AL, USA
Language: English
Abstract: In multilevel structures on monolithic **integrated circuits**, the metal layers most frequently used are pure aluminium or aluminium alloys, and in general these metal **layers** are **insulated** from one another by a dielectric, typically CVD deposited **silicon dioxide** or phosphosilicate glass. For VLSI application where interconnect dimensions are scaled, these dielectrics suffer from step coverage integrity, defect densities, and fine patterning of the second aluminium layer. **Polyimide** has been investigated as a suitable dielectric using a double layer metal test mask developed at NASA/MSFC.

Indications to date are that **polyimides** render an excellent substitute for the SiO/sub 2/ and can be processed almost exclusively using wet processing techniques.
Subfile: B

18/3,AB/10
DIALOG(R)File 2:INSPEC

01495910 INSPEC Abstract Number: B80018976
Title: Single photoresist for **polyimide**-insulator via
Author(s): Agnihotri, R.K.; Chiu, G.T.; Johnson, C., Jr.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.5 p.1821-2
Publication Date: Oct. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: Vias formed through **polyimide** and **insulator layers**, such as **quartz** or Si/sub 3/N/sub 4/, require two photoresist layers to open a large **polyimide** window and a smaller insulator window. A single photoresist layer is used for etching both windows for vias between metal layers.
Subfile: B

18/3,AB/11
DIALOG(R)File 2:INSPEC

01289112 INSPEC Abstract Number: B79004060
Title: Removing dual **insulating layers** over a metallic layer
Author(s): Rapoport, N.R.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.20, no.8 p.3004-5
Publication Date: Jan. 1978 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: A technique for selectively and rapidly removing dual **insulating layers**, such as **polyimide** and **quartz** from a portion of a metallic layer, e.g. copper-doped Al, utilises a vibrating probe needle connected, if desired, to an appropriate electrical contact indicating circuit. This technique may be employed when characterisation or failure analysis of a circuit is desired without causing damage to the Al layer.

24/3,AB/1
DIALOG(R)File 2:INSPEC

7314515 INSPEC Abstract Number: B2002-08-0170J-073
Title: Adhesion characteristics of underfill material with various package components after plasma and UV/ozone treatments
Author(s): Man-Lung Sham; Mei Lam; Jang-Kyo Kim
Author Affiliation: Dept. of Mech. Eng., Hong Kong Univ. of Sci. & Technol., China
Conference Title: Advances in Electronic Materials and Packaging 2001 (Cat. No.01EX506) p.208-15
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xviii+449 pp.
ISBN: 0 7803 7157 7 Material Identity Number: XX-2002-00448
U.S. Copyright Clearance Center Code: 0-7803-7157-7/01/$10.00
Conference Title: Advances in Electronic Materials and Packaging 2001
Conference Sponsor: Korea Sci. & Eng. Found.; Korea Res. Found.; IMAPS-Korea; Samsung Electron.; LG Electron.; Hynix Semicond.; Amkor Technol.; MTS-Korea; Hong Kong Univ. Sci. & Technol.; US Army Res. Office-Far East; Korea-Japan Core Univ. Program
Conference Date: 19-22 Nov. 2001 Conference Location: Jeju Island, South Korea
Language: English
Abstract: The role of underfill in enhancing the reliability of flip **chip** packages is of paramount importance, particularly for the low-cost packages made of organic printed circuit boards. Amongst many reliability issues in flip **chip** packages, delamination between the underfill and other package components is detrimental to the mechanical and functional performance of the package because delamination often leads to premature failure of the whole device. In the present study, the interfacial bond strengths of both conventional and no-flow underfill resins with **die passivation**, solder, and **polyimide** soldermask are measured based on the button shear test; and the surface characteristics of these substrates are analysed using several analytical tools, including atomic force microscopy, X-ray photoelectron spectroscopy and contact angle measurement. Plasma and UV/ozone treatments are applied before encapsulation to improve the underfill-package component interface bond. It is found that the interfacial bond strength of underfill with solder was the weakest, while it was highest with **silicon nitride passivation** layer amongst the above substrates studied.
Both plasma and UV/ozone treatments improved the interfacial bond strength with **polyimide** soldermask along with a decrease in contact angle of the surface. Among the various thermodynamic parameters the spreading coefficient was shown to have close correlation with the underfill-solder interfacial bond strength. The significance of this finding is discussed.
Subfile: B

24/3,AB/2
DIALOG(R)File 2:INSPEC

7251581 INSPEC Abstract Number: B2002-06-0170J-014
Title: Adhesion of underfill and components in flip **chip** encapsulation
Author(s): Lianhua Fan; Kyoung-Sik Moon; Wong, C.P.

Author Affiliation: Packaging Res. Center, Georgia Inst. of Technol., Atlanta, GA, USA
Journal: Journal of Adhesion Science and Technology vol.16, no.2 p. 213-23
Publisher: VSP,
Publication Date: 2002 Country of Publication: Netherlands
CODEN: JATEE8 ISSN: 0169-4243
SICI: 0169-4243(2002)16:2L.213:AUCF;1-0
Material Identity Number: J712-2002-004
Language: English
Abstract: The underfill material is a polymeric adhesive used in flip **chip** packaging. It encapsulates the solder joints by filling the gap between a silicon **die** and an organic substrate or board. Within a typical flip **chip** structure, there are interfaces between the various components, namely, substrate, solder mask, flux residue, underfill encapsulant and **die passivation** layer, etc. Maintaining a good adhesion condition, both as-made and after temperature/humidity aging, is vital for these interfaces because of the expected performance of the flip **chip** device, where the underfill material is employed to enhance the flip **chip** interconnect reliability. We have studied the adhesion strength between the various components for different process variables as measured with the lap shear and **die** shear test configurations. The effects of the assembly factors, i.e. solder mask, flux residue, underfill, and **die passivation** , etc., were evaluated and the adhesion strength was found to depend greatly on these factors. The **die** shear strength of a **passivated die** assembled on an organic board coated with a solder mask was much higher after using a no-clean flux on the solder mask than for assembly without such a no-clean flux. The influence of some accelerated aging tests on adhesion durability was also investigated. A benzocyclobutene **die passivation** layer exhibited better capability in retaining **die** shear strength than a **silicon nitride** or **polyimide passivation** layer, especially for the initial aging period. The knowledge obtained in this study should provide insights into interfacial adhesion in the flip **chip** assembly structure.
Subfile: B

24/3,AB/3
DIALOG(R)File 2:INSPEC

7068547 INSPEC Abstract Number: B2001-11-0170J-253
Title: Surface property of **passivation** and solder mask for flip **chip** packaging
Author(s): Shijian Luo; Wong, C.P.
Author Affiliation: Sch. of Mater. Sci. & Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: 2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220) p.1350-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xxxiii+1518 pp.
ISBN: 0 7803 7038 4 Material Identity Number: XX-2001-01138
U.S. Copyright Clearance Center Code: 0 7803 7038 4/2001/$10.00
Conference Title: 51st Electronic Components and Technology Conference 2001. Proceedings
Conference Sponsor: Components, Packaging, & Manuf. Technol. (CPMT) Soc. IEEE; Electron. Components Assemblies & Mater. Assoc. (ECA); Electron.

Components Sector of the Electron. Ind. Alliance
Conference Date: 29 May-1 June 2001 Conference Location: Orlando, FL, USA
Language: English
Abstract: Adhesion of underfill to **passivation** and solder mask is critical to the reliability of an underfilled flip **chip** package. In this study, the surface properties of solder mask and four **passivation** materials: benzocyclobutene (BCB), **polyimide** (PI), silicon oxide (SiO/sub 2/), and **silicon nitride** (SiN), along with their respective preparation procedures were investigated. A combination of both wet and dry cleaning processes was very effective to remove contaminants from the surface. The oxygen atom, introduced during O/sub 2/ plasma treatment or UV/O/sub 3/ treatment, led to the increase of the base component of surface tension. X-ray photoelectron spectroscopy (XPS) experiments confirmed the increase of oxygen concentration at the surface after UV/O/sub 3/ treatment. Wetting of underfill on **passivation** and solder mask was slightly improved at higher temperatures. Although UV/O/sub 3/ cleaning and O/sub 2/ plasma treatment significantly improved the wetting of underfill on **passivation** materials, they did not improve adhesion strength of epoxy underfill to **passivation**. Therefore, the wetting was not the controlling factor in adhesion of the system studied.
Subfile: B

24/3,AB/4
DIALOG(R)File 2:INSPEC

7068298 INSPEC Abstract Number: B2001-11-0170J-242
Title: Adhesion of flip-**chip** underfills to various **die passivations** before and after accelerated environmental exposure
Author(s): Dimke, M.
Author Affiliation: Dexter Electron. Mater., Olean, NY, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.71-5
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2001 Country of Publication: USA 520 pp.
Material Identity Number: XX-2000-03037
Conference Title: Proceedings of 6th Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: IMAPS; ITRI; Japan Inst. Electron. Packaging, Semicond. Equipment & Mater. Int.; et al
Conference Date: 13-16 Feb. 2001 Conference Location: Kauai, HI, USA
Language: English
Abstract: With the ever increasing reliability requirements and price pressures of electronic packages, it is more important than ever to understand fundamental failure modes in packages. Since delamination of the flip-**chip** underfill to the **die passivation** is the most common failure mechanism in flip-**chip** packages, this study examines the performance of various flip-**chip** underfills with the three most common **die passivations**, benzocyclobutene (BCB), **polyimide** and **silicon nitride** . It has been shown that measuring adhesion values for underfills to **passivations** strongly correlates to overall flip-**chip** package reliability. There is therefore great value in knowing the adhesion of various flip-**chip** underfills to the **passivations** and how that adhesion is maintained over the course of a rigorous but typical set of reliability requirements.

This study evaluates adhesion between flip-**chip** underfill and **passivation** using a **die** shear methodology. The test vehicle used for this study is a 100-mil square peripherally bumped **die** provided by Flipchip Technologies. The dice are identical with the exception of the three **passivations** being examined. Six different underfills were evaluated for adhesion after the listed environmental exposures; initial, JEDEC 3 using a 260 C reflow, JEDEC 3 plus 24 hr. pressure cooker test (PCT), JEDEC 3 plus 96 hr. PCT, JEDEC 3 plus 168 hr. PCT, and JEDEC 3 plus 1000 cycles condition B. Results of the study show **passivation** /underfill combinations with good adhesion under environmental exposure. The study also chronicles adhesion evolution in underfill materials.

Subfile: B

24/3,AB/5

DIALOG(R)File 2:INSPEC

7049078 INSPEC Abstract Number: B2001-11-0170J-018

Title: Influence of temperature and humidity on adhesion of underfills for flip **chip** packaging

Author(s): Shijian Luo; Wong, C.P.

Author Affiliation: Sch. of Mater. Sci. & Eng., Georgia Inst. of Technol., Atlanta, GA, USA

Conference Title: 2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220) p.155-62

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2001 Country of Publication: USA xxxiii+1518 pp.

ISBN: 0 7803 7038 4 Material Identity Number: XX-2001-01138

U.S. Copyright Clearance Center Code: 0 7803 7038 4/2001/$10.00

Conference Title: 51st Electronic Components and Technology Conference 2001. Proceedings

Conference Sponsor: Components, Packaging, & Manuf. Technol. (CPMT) Soc. IEEE; Electron. Components Assemblies & Mater. Assoc. (ECA); Electron. Components Sector of the Electron. Ind. Alliance

Conference Date: 29 May-1 June 2001 Conference Location: Orlando, FL, USA

Language: English

Abstract: This paper systematically discusses the influence of temperature and humidity on the adhesion performance of underfill material (epoxy cured with acid anhydride), evaluated by **die** shear test after exposure to various conditions. The adhesion strength between the underfill and **passivation** is not affected significantly by thermal cycling between -55 degrees C and 125 degrees C for 1000 cycles. The adhesion strength of underfill material decreases with the increase of test temperature above room temperature, due to the decrease of modulus of the underfill with the increase of temperature. A sharp decrease in adhesion strength occurs as temperature increase towards the glass transition temperature of the underfill material. Adhesion strength of underfill with different **passivation** materials decreases after aging in a high temperature and high humidity environment. The extent of this decrease is dependent on the chemistry of underfill formulation and the hydrophilicity of the **passivation** material. Hydrophilic **passivation** such silicon oxide (SiO/sub 2/) and **silicon nitride** (SiN) shows much more severe adhesion degradation than hydrophobic **passivation** such as benzocyclobutene (BCB) and **polyimide** (PI). Adhesion degradation kinetics is discussed in terms of mobility of polymer chains and of

absorbed water. The adhesion stability for hydrophilic **passivation** can be successfully improved by use of a coupling agent such as silane that introduces stable chemical bond at interface.
Subfile: B

24/3,AB/6
DIALOG(R)File 2:INSPEC

6944284 INSPEC Abstract Number: B2001-07-0170J-054
Title: Study on surface tension and adhesion for flip **chip** packaging
Author(s): Shijian Luo; Harris, T.; Wong, C.P.
Author Affiliation: Packaging Res. Center, Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: Proceedings International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (IEEE Cat. No.01TH8562) p.299-304
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA ix+414 pp.
ISBN: 0 930815 64 5 Material Identity Number: XX-2001-00699
Conference Title: Proceedings International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces
Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol (CPMT); Georgia Inst. Technol., Packaging Res. Center (PRC)
Conference Date: 11-14 March 2001 Conference Location: Braselton, GA, USA
Language: English
Abstract: In a flip **chip** package with underfill, adhesion of underfill to **passivation** and solder mask is critical to the reliability of the assembly. In this study, the three-liquid-probe method was used to investigate the surface properties of the solder mask and four different **passivation** materials, benzocyclobutene (BCB), **polyimide** (PI), silicon oxide (SiO/sub 2/), and **silicon nitride** (Si/sub 3/N/sub 4/), after different preparation procedures. A combination of both wet and dry clean processes was very effective for removal of contaminants from the surface. The oxygen atom, introduced during O/sub 2/ plasma treatment or UV/O/sub 3/ treatment, led to an increase of the base component of surface tension. X-ray photoelectron spectroscopy (XPS) experiments confirmed the increase of surface oxygen concentration after UV/O/sub 3/ treatment. Wetting of underfill on **passivation** and solder mask was slightly improved at higher temperatures. Although UV/O/sub 3/ cleaning and O/sub 2/ plasma treatment significantly improved the wetting of underfill on **passivation** materials, they did not show improvement in adhesion strength. As such, the wetting was not the controlling factor in adhesion of the system studied.
Subfile: B

24/3,AB/7
DIALOG(R)File 2:INSPEC

6802844 INSPEC Abstract Number: B2001-02-8520B-005
Title: Qualification of a spin apply, photodefinable polymer for packaging of automotive circuits

Author(s): Wyant, J.L.; Schuckert, C.C.
Author Affiliation: Delphi Delco Electron. Syst., Kokomo, IN, USA
Journal: Solid State Technology vol.43, no.11 p.125-6, 128, 130
Publisher: PennWell Publishing,
Publication Date: Nov. 2000 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
SICI: 0038-111X(200011)43:11L.125:QSAP;1-U
Material Identity Number: S046-2000-011
Language: English
Abstract: Spin apply polymer coatings can be used in packaging applications as a stress buffer **passivation** layer for improved device reliability. They can also serve as dielectric and **passivation** layers in bond pad redistribution circuits for flip-**chip** packaging. A high T/sub g/ photodefinable **polyimide** was selected for both applications, due to good chemical resistance and desirable adhesion characteristics to **silicon nitride** , various molding compounds, aluminum, and to itself. The product exhibited a wide process window, and tapered via slopes were obtained for metallization through minor process modifications.
Subfile: B

24/3,AB/8
DIALOG(R)File 2:INSPEC

6734576 INSPEC Abstract Number: B2000-11-2560J-019
Title: Investigation of process related reliability for InP-based heterojunction bipolar transistors (HBTs)
Author(s): Kiziloglu, K.; Thomas, S., III; Paine, B.M.; Williams, F., Jr; Fields, C.H.
Author Affiliation: HRL Labs., Malibu, CA, USA
Conference Title: Proceedings of the State-of-the-Art Program on Compound Semiconductors (SOTAPOCs XXX) (Electrochemical Society Proceedings Vol.99-4) p.95-102
Editor(s): Abernathy, C.R.; Baca, A.; Buckley, D.N.; Chen, K.H.; Kopf, R. ; Sah, R.E.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA viii+264 pp.
ISBN: 1 56677 226 5 Material Identity Number: XX-2000-00259
Conference Title: State-of-the Art Program on Compound Semiconductors XXX
Conference Sponsor: Electrochem. Soc
Conference Date: 2-7 May 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: Life tests were performed on discrete AlInAs-GaInAs-InP heterojunction bipolar transistors (HBTs) at junction temperatures (T/sub j/) of 200 to 230 degrees C and bias conditions of V/sub CE/=3 V and J/sub C/=23 kA/cm/sup 2/. Devices from multiple **wafers** were tested to investigate the effects of growth temperature and a **silicon nitride** process step on device reliability. **Wafers** were grown by molecular beam epitaxy (MBE) at two different temperatures. In half of the **wafers** in the experiment, a SiN/sub x/ layer was used as a mask for base-collector mesa etch and removed afterwards. In the other half, the etch was performed using a photoresist mask. All of the transistors were subsequently **passivated** by **polyimide**. Whereas a small change in the MBE growth temperature did not directly affect device characteristics or reliability, the presence of process steps involving SiN/sub x/ had a measurable effect on device characteristics after bias and temperature stress. In devices processed with the SiN/sub x/ steps, an increase in the

base-emitter turn-on voltage (V/sub BE/) was observed. For these devices, a failure criterion of 5% increase in V/sub BE/ results in an activation energy (E/sub a/) of 1.48 eV and an expected median time to failure (MTTF) of 2.1*10/sup 6/ hr at T/sub j/=125 degrees C.
Subfile: B

24/3,AB/9
DIALOG(R)File 2:INSPEC

6430680 INSPEC Abstract Number: B2000-01-1350H-022, C2000-01-7410D-100
Title: Design and fabrication of GaAs microwave monolithic **integrated circuits** using 0.2 mu m GMMT PHEMT foundry process
Author(s): Majlis, B.Y.; Ariffin, A.; Mat, A.F.A.; Jaafar, S.; Bujang, S. ; Yahya, M.R.
Author Affiliation: Fac. of Eng., Kebangsaan Malaysia Univ., Bangi, Malaysia
Conference Title: ICSE'98. 1998 IEEE International Conference on Semiconductor Electronics. Proceedings (Cat. No.98EX187) p.229-31
Editor(s): Shaari, S.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA ix+259 pp.
ISBN: 0 7803 4971 7 Material Identity Number: XX-1999-02040
U.S. Copyright Clearance Center Code: 0 7803 4971 7/98/$10.00
Conference Title: Proceedings ICSE'98. 1998 IEEE International Conference on Semiconductor Electronics. Proceedings
Conference Sponsor: IEEE Electron Devices Soc.; Univ. Kebangsaan Malaysia
Conference Date: 24-26 Nov. 1998 Conference Location: Bangi, Malaysia
Language: English
Abstract: Summary form only given. A number of MMICs with operating frequencies from L to X band have been designed and fabricated using the GMMT foundry. All circuits were designed using MMIC CAD Series IV Libra on PC and workstation. The circuit functions include a range of TWAs, LNAs, wide band amplifiers, switches, mixers, oscillators, four bit attenuators, phase shifters and power amplifiers. Fabrication was conducted on 3" GaAs **wafers** using the GMMT PHEMT process, with 0.3 mu m gate length, via holes through the substrate, MIM nitride and **polyimide** capacitors and is fully protected by **silicon nitride passivation**. The primary applications of GaAs high electron mobility transistor (HEMT) circuits are in satellite receivers, consumer video applications, high frequency scanners, wireless LAN and other low noise front ends. Most of the operating frequencies for this application are in the range from 1 to 15 GHz.
Subfile: B C

24/3,AB/10
DIALOG(R)File 2:INSPEC

5684108 INSPEC Abstract Number: B9710-2560J-029
Title: **Passivation** of InP-based HBTs for high bit rate circuit applications
Author(s): Caffin, D.; Bricard, L.; Courant, J.L.; How Kee Chun, L.S.; Lescaut, B.; Duchenois, A.M.; Meghelli, M.; Benchimol, J.L.; Launay, P.
Author Affiliation: Lab. de Bagneux, CNET, Bagneux, France

Conference Title: Conference Proceedings. 1997 International Conference on Indium Phosphide and Related Materials (Cat. No.97CH36058) p.637-40
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA xii+680 pp.
ISBN: 0 7803 3898 7 Material Identity Number: XX97-01229
U.S. Copyright Clearance Center Code: 0 7803 3898 7/97/$10.00
Conference Title: Conference Proceedings. 1997 International Conference on Indium Phosphide and Related Materials
Conference Sponsor: IEEE Lasers & Electro-Opt. Soc.; IEEE Electron Devices Soc
Conference Date: 11-15 May 1997 Conference Location: Cape Cod, MA, USA
Language: English
Abstract: We have studied different materials (**silicon nitride**, silicon oxide, **polyimide**) for **passivating** InP-based HBTs, and their influence on the device electrical performances. **Polyimide** was found to induce the least degradation after **passivation** . A double heterojunction InP/InGaAs HBT fabrication process, including **polyimide passivation** and planarization, has been assembled, allowing us to realize high bit-rate circuits, such as a 36 Gb/s 2:1 multiplexer.
Subfile: B

24/3,AB/11
DIALOG(R)File 2:INSPEC

04199078 INSPEC Abstract Number: B9209-0170J-007
Title: Hermetic **passivation** of **chip**-on-board circuits
Author(s): Gates, L.E.; Bakhit, G.G.; Ward, T.G.; Kubacki, R.M.
Author Affiliation: Hughes Aircraft Co., Los Angeles, CA, USA
Conference Title: 1991 Proceedings. 41st Electronic Components and Technology Conference (Cat. No.91CH2989-2) p.813-19
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA xvi+901 pp.
ISBN: 0 7803 0012 2
U.S. Copyright Clearance Center Code: 0569-5503/91/0000-0813$01.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 11-16 May 1991 Conference Location: Atlanta, GA, USA
Language: English
Abstract: Results of a screening study and evaluation of **silicon nitride**, silicon dioxide, and a combination of the two as **passivation** for **integrated circuit** assemblies are presented. Screening test samples consisted of silicon **wafers** coated with various combinations of aluminum and spun-on **polyimide**. A series of chemical, mechanical, and environmental tests was carried out. The **passivation** coatings were applied by four different vendors using CVD (chemical vapor deposition), plasma-enhanced CVD, and room-temperature reactive plasma. The most promising material was then applied to a variety of more complex samples, including triple track resistor assemblies, and active **integrated circuits** which were electrically tested to evaluate results. **Silicon nitride** at a nominal thickness of 5000 AA applied by the room-temperature reactive plasma process was judged to be the best **passivation** material.
Subfile: B

24/3,AB/12

DIALOG(R)File 2:INSPEC

03743160 INSPEC Abstract Number: B90069323
Title: Corrosion of aluminum interconnect **passivated** with **polyimide** or **silicon nitride**
Author(s): Comizzoli, R.B.; Opila, R.L.; Wong, Y.H.
Author Affiliation: AT&T Bell Lab., Murray Hill, NJ, USA
Conference Title: Electronic Packaging Materials Science IV. Symposium p.277-82
Editor(s): Jaccodine, R.; Jackson, K.A.; Lillie, E.D.; Sundahl, R.C.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1989 Country of Publication: USA xiii+494 pp.
Conference Sponsor: Army Res. Office; Allied-Signal Corp.; Amoco; Dow; Intel; Office Naval Res
Conference Date: 24-28 April 1989 Conference Location: San Diego, CA, USA
Language: English
Abstract: The corrosion rate of sputtered aluminum test patterns **passivated** with either PI or plasma-deposited **silicon nitride** (SiN) was measured at 85 degrees C and 85% relative humidity (RH). The objectives of the work were to: assess the failure rates of biased aluminum interconnection with PI or SiN **passivation**; determine the failure mechanisms in each case; and evaluate the suitability of PI **passivation** for high voltage **ICs** in non-hermetic packages. In this report, the test device fabrication and evaluation procedures are first described. Then the results are presented, including both the failure rate measurements and the failure analyses. Finally, the results are compared and discussed.
Subfile: B

24/3,AB/13
DIALOG(R)File 2:INSPEC

03720447 INSPEC Abstract Number: B90061467
Title: Corrosion of aluminum interconnect **passivated** with **polyimide** or **silicon nitride**
Author(s): Comizzoli, R.B.; Opila, R.L.; Wong, Y.H.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Conference Title: Interfaces Between Polymers, Metals and Ceramics Symposium p.205-10
Editor(s): DeKoven, B.M.; Gellman, A.J.; Rosenberg, R.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1989 Country of Publication: USA xiii+426 pp.
Conference Date: 25-27 April 1989 Conference Location: San Diego, CA, USA
Language: English
Abstract: The corrosion rate of sputtered aluminum test patterns **passivated** with either PI or plasma-deposited **silicon nitride** (SiN) was measured at 85 degrees C and 85% relative humidity (RH). The objectives of this work were to: assess the failure rates of biased aluminum interconnection with PI or SiN **passivation**; determine the failure mechanisms in each case; and, as a result, evaluate the suitability of PI **passivation** for high voltage **ICs** in non-hermetic packages. The test device fabrication and evaluation procedures are first described. Then the results are presented, including both the failure rate measurements and the failure analyses. Finally, the

results are compared and discussed.
Subfile: B

24/3,AB/14
DIALOG(R)File 2:INSPEC

02759787 INSPEC Abstract Number: B86062283
Title: **Polyimide** -substrate bonding studies using gamma -aminopropyltriethoxysilane coupling agent
Author(s): Anderson, H.R., Jr.; Khojasteh, M.M.; McAndrew, T.P.; Sachdev, K.G.
Author Affiliation: IBM Corp., Hopewell Junction, NY, USA
Conference Title: 36th Electronic Components Conference Proceedings 1986 (Cat. No.86CH2302-8) p.331-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1986 Country of Publication: USA 684 pp.
U.S. Copyright Clearance Center Code: 0569-5503/86/0000-0331$01.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 5-7 May 1986 Conference Location: Seattle, WA, USA
Language: English
Abstract: Application of **polyimides** in **microelectronics** fabrication for interlevel dielectric, **passivation** or device isolation requires that the polymer films maintain interface integrity with a variety of surfaces at high temperature and during solvent processing. gamma -aminopropyltriethoxysilane (gamma -APS) in aqueous solution is the most commonly used adhesion promoter for bonding of **polyimides** to inorganic substrates including silicon oxide, **silicon nitride** and ceramic. This study is concerned with the adhesion of pyromellitic dianhydride-oxydianiline (PMDA-ODA) derived **polyimide** films on gamma -APS-treated silicon oxide and **silicon nitride** surfaces under high temperature processing. Using the standard 90 degrees peel test for adhesion measurements, it is shown that polymer-substrate interface stability is completely maintained even after multiple thermal cycles with 25 degrees to 375 degrees to 25 degrees C excursions in nitrogen and in forming gas ambients.
Subfile: B

24/3,AB/15
DIALOG(R)File 2:INSPEC

02725384 INSPEC Abstract Number: B86052319
Title: Reliability evaluation of plastic packaged devices for long life applications by THB test
Author(s): Brambilla, P.
Author Affiliation: Reliability & Quality, Dept. of Telettra S.p.A, Milano, Italy
Journal: Microelectronics and Reliability vol.26, no.2 p.365-84
Publication Date: 1986 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
U.S. Copyright Clearance Center Code: 0026-2714/86$3.00+.00
Language: English
Abstract: The reliability of transistors, bipolar and CMOS **integrated circuits** encapsulated in different types of plastic packages was investigated using the 85 degrees C/85% RH test with applied bias and the results compared with a long term operating life test.

Particular attention was devoted to pointing out the influence of technology, process control and working conditions on device reliability and failure mechanisms. In micropackaged transistors the importance of surface **passivation** in protecting the devices against gold corrosion was especially considered, while the need of good process control was confirmed by the results of the test on micropackaged linear **integrated circuits**. In dual-in-line CMOS **integrated circuits silicon nitride** and **polyimide** give, in general, a superior protection, but good results were obtained also with normal P-glass **passivation** when a clever arrangement of layout design rules was adopted. Results obtained exhibit a significant improvement in the reliability of plastic packaged devices, with the best figures showing no failures after 15000 hours at 85 degrees C/85% RH test with bias.
Subfile: B

24/3,AB/16
DIALOG(R)File 2:INSPEC

02617101 INSPEC Abstract Number: B86014229
Title: Failure analysis of ECL memories by means of voltage contrast measurements and advanced preparation techniques
Author(s): Dallman, A.; Menzel, G.; Weyl, R.; Fox, F.
Author Affiliation: Siemens AG, Munchen, West Germany
Conference Title: 23rd Annual Proceedings Reliability Physics 1985 (Cat. No. 85CH2113-9) p.224-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA viii+252 pp.
U.S. Copyright Clearance Center Code: CH2113-9/85/0000-0224$01.00
Conference Sponsor: IEEE
Conference Date: 26-28 March 1985 Conference Location: Orlando, FL, USA
Language: English
Abstract: After 4-6 weeks of testing, a number of the computer installed ECL memories showed defects. Previous electrical characterization of the burned devices, also after their mounting on printed boards, had revealed no detectable failures. To analyze the failures, the ceramic housings of some memories were opened with a diamond saw and the protection layer of **polyimide** as well as the **silicon nitride passivation** layer were removed by means of heated nitric acid and CF/sub 4/ plasma etching, respectively. The Al fingers are the only visible structural irregularities in the devices. Since the fingers occur in both the intact and the defect cells, it is believed that there must be additional defects in the isolation oxide. The results of the voltage contrast measurements, in conjunction with the effects arising from the elimination of the Al fingers, are seen as giving clear evidence for oxide defects.
Subfile: B

24/3,AB/17
DIALOG(R)File 2:INSPEC

02409590 INSPEC Abstract Number: B85018476
Title: Nitride/polyamide isolation enhancement
Author(s): Leipold, W.C.; Motsiff, W.T.; Rath, P.C.
Author Affiliation: IBM Corp., Armonk, NY, USA

Journal: IBM Technical Disclosure Bulletin vol.27, no.4A p.2086-7
Publication Date: Sept. 1984 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: In this enhanced process for fabricating dual-dielectric nitride/**polyimide** **passivated** IGFET devices the **silicon** **nitride** layer is made much thinner than it is in conventional devices of this type and is entirely covered by a thin **polyimide** layer that is formed prior to the formation of the usual thicker **polyimide** layer, which only partially overlies the nitride layer.
Subfile: B

24/3,AB/18
DIALOG(R)File 2:INSPEC

02109391 INSPEC Abstract Number: B83049285
Title: Plastic encapsulated GaAs MESFET
Author(s): Wetzel, C.; Frary, J.
Author Affiliation: Motorola Inc., Schaumburg, IL, USA
Journal: Motorola Technical Developments vol.3 p.72
Publication Date: March 1983 Country of Publication: USA
CODEN: MTDEDP ISSN: 0887-5286
Language: English
Abstract: Describes a gallium arsenide depletion-mode low-noise MESFET which is **passivated** with a Dupont **polyimide** and encapsulated in a plastic package. The process employs Dupont P12545 **polyimide** as the **passivation** layer, epoxy **die** attach to a Macro-X leadframe, and encapsulation with Hysol 130 resin. Studies have shown that neither the **polyimide** nor the plastic packaging degrades the device RF performance, while **silicon** **nitride** does. This process also offers the advantages of lower cost and easier fabrication.
Subfile: B

24/3,AB/19
DIALOG(R)File 2:INSPEC

01951453 INSPEC Abstract Number: B82059441
Title: A manufacturing process for analog and digital gallium arsenide **integrated** **circuits**
Author(s): Van Tuyl, R.L.; Kumar, V.; D'Avanzo, D.C.; Taylor, T.W.; Peterson, V.E.; Hornbuckle, D.P.; Fisher, R.A.; Estreich, D.B.
Author Affiliation: Hewlett-Packard Co., Santa Rosa Technol. Centre, Santa Rosa, CA, USA
Journal: IEEE Transactions on Microwave Theory and Techniques vol.MTT-30, no.7 p.935-42
Publication Date: July 1982 Country of Publication: USA
CODEN: IETMAB ISSN: 0018-9480
Conference Title: 1981 IEEE GaAs Integrated Circuits Symposium
Conference Date: 27-29 Oct. 1981 Conference Location: San Diego, CA, USA
Language: English
Abstract: A process for manufacturing small-to-medium scale GaAs **integrated** **circuits** is described. Integrated FETs, diodes, resistors, thin-film capacitors, and inductors are used for monolithic integration of digital and analog circuits. Direct implantation of Si into

>10/sup 5/ Omega .cm resistivity substrates produces n-layers with +or-10-percent sheet resistance variation. A planar fabrication process featuring retained anneal cap (SiO/sub 2/), proton isolation, recessed Mo-Au gates, **silicon nitride passivation** , and a dual-level metal system with **polyimide** intermetal dielectric is described. Automated on-**wafer** testing at frequencies up to 4 GHz is introduced, and a calculator-controlled frequency domain test system is described. Circuit yields for six different circuit designs are reported, and process defect densities are inferred.
Subfile: B

24/3,AB/20
DIALOG(R)File 2:INSPEC

01180340 INSPEC Abstract Number: B78019152
Title: **Passivation** coatings for thin film resistors
Journal: Circuits Manufacturing vol.17, no.8 p.16, 18, 22, 24
Publication Date: Aug. 1977 Country of Publication: USA
CODEN: CMFGAF ISSN: 0009-7306
Language: English
Abstract: In the past, hybrid manufacturers applied **passivation** coatings to thin film nichrome resistors on the theory that the coating improved the stability of the resistors. Silicon monoxide represented the most frequently used coating, with glass coatings sometimes used for thin film resistors on silicon **chips** . Researchers at National Semiconductor, Santa Clara, CA, studied various alternative coatings (silicon dioxide, borosilicate glass, **silicon nitride** and **polyimide**) to determine their effect on resistor stability. They also conducted humidity tests to determine if these coatings could protect nichrome resistors from galvanic corrosion as well as afford mechanical protection. These experiments are described and results given.

FILE WPIX JAPIO
E US6352940/PN
L1 868176 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(W)(CIRCUIT? OR CHIP OR ELECTRONIC?) OR CHIP OR MICROCIRCUIT? OR DIE OR DICE OR LOGIC(W) CIRCUIT? OR WAFER OR MICROELECTRONIC?
L2 332744 S (SILICON OR SI)(W)(DIOXIDE OR O2) OR SILICA## OR SILICATE OR KEATITE OR HYALITE OR LECHATELIERITE OR QUARTZ OR SIDERITE OR SIFRACO OR CHALCEDONY OR QUARTZINE OR CRISTOBALITE OR COESITE OR STISHOVITE OR CHRYSOPRASE OR SIO2
L3 2309 S (SILICON OR SI)(W)(OXYNITRIDE) OR DISILICON OR OXYNITRIDE OR SILICON OXIDE(N) NITRIDE OR SI2ON2
L4 46789 S (SILICON OR SI3)(W)(NITRIDE OR N4) OR SI3N4 OR BAYSINID OR DENKA OR ROYDAZIDE OR NIERITE
L5 420385 S (INSULAT? OR OXIDE OR DIELECTRIC)(2N)(LAYER? OR FILM OR COAT####)
L6 2800352 S ADHESI? OR ADHERE? OR STICK? OR CLING? OR BOND? OR CEMENT? OR CONGLUTIN? OR AGGLUTIN? OR MUCILAG? OR TACK? OR GLUE? OR GLUING# OR PASTE? OR PASTING# OR GUM? OR HOLD? OR GRIP? OR GRASP? OR BIND?
L7 37389 S L2 AND L5
L8 328 S L3 AND L6
L9 1278 S L4 AND PASSIVAT?
L10 6151 S L1 AND L7
L11 83 S L10 AND L9
L12 2 S L11 AND L8
L13 12 S L11 AND POLYIMIDE
L14 11 S L13 NOT L12
L15 3528 S L1 AND PASSIVAT?
L16 274 S L15 AND L7
L17 3 S L16 AND L8
L18 1 S L17 NOT (L12 OR L13)
L19 20 S L15 AND L8
L20 17 S L19 NOT (L12 OR L13 OR L17)
L21 337 S L15 AND POLYIMIDE
L22 44 S L21 AND L2
L23 18 S L22 AND L4
L24 3 S L22 AND L3
L25 5 S (L23 OR L24) NOT (L12 OR L13 OR L17 OR L19)

L26 70 S L11 NOT (L12 OR L13 OR L17 OR L19 OR L23 OR L24)

L12 ANSWER 1 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 2001-137243 [14] WPIX
DNN N2001-099933 DNC C2001-040177
TI Formation of laser accessible fuse for memory arrays by forming fuse with rupture zone, patterning metal layer to form conductive wiring connected to conductive contacts, plate over rupture zone, and wiring pad, patterning **passivation** layer.
DC L03 U11 U13 U14
IN LIN, H; TZENG, W; YANG, C
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 6180503 B1 20010130 (200114)* 17p
ADT US 6180503 B1 US 1999-354852 19990729
PRAI US 1999-354852 19990729
AB US 6180503 B UPAB: 20010312

NOVELTY - A laser accessible fuse is formed by forming a fuse with a rupture zone; patterning a metal layer to form conductive wiring connected to at least two conductive contacts, a plate over the rupture zone, and a wiring pad; patterning a **passivation** layer by anisotropically etching the **passivation** layer and an anti-reflective coating over a **bonding** pad, forming a laser access window.

DETAILED DESCRIPTION - A laser accessible fuse is formed by:

(a) depositing a layer of fusible material on a first **insulative layer** on a silicon **wafer** (70);

(b) patterning the layer of fusible material to form a fuse (78) with a rupture zone (78A);

(c) depositing a second **insulative layer** over the **wafer**;

(d) forming conductive contacts to the fuse through openings in the second **insulative layer**, where the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(e) depositing a first metal layer (94) on the second **insulative layer**;

(f) patterning the first metal layer to form conductive wiring (96) connected to each of at least two conductive contacts, a plate (86) over the rupture zone, and a wiring pad;

(g) depositing a third **insulative layer** over the **wafer**;

(h) patterning the third **insulative layer** to form a via opening to the wiring pad, and a window opening over the rupture zone;

(i) depositing a second metal layer (108) on the **wafer**;

(j) depositing an anti-reflective coating (92) on the second metal layer;

(k) patterning a **bonding** pad in the second metal layer over the via opening and removing the anti-reflective coating, the second metal layer, and the first metal layer in the window opening;

(l) depositing a **passivation** layer over the **wafer** ; and

(m) patterning the **passivation** layer by anisotropically etching the **passivation** layer and the anti-reflective coating over the **bonding** pad while simultaneously etching a region within the window opening, penetrating the second **insulative layer** to a final second **insulative layer** thickness over the rupture zone, forming a laser access window.

USE - For forming a laser accessible fuse for memory arrays useful in computer memory **chips**, e.g., dynamic random access memory

(DRAM).
ADVANTAGE - The invention (a) allows for a simultaneous etching of the **passivation** layer and **bonding** pad openings; (b) retards fuse access opening formation during via formation using the transient etch stop layers; (c) improves the uniformity of **insulative layers** over fuse links while at the same time over-etches vias and **passivation** layer access openings to thoroughly remove anti reflection coating layers; and (d) uses a single photolithographic mask for patterning a **passivation** layer to form access to **bonding** pads and laser access openings.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a DRAM with a fuse access window formed.

Wafer 70
Fuse 78
Rupture zone 78A
Plate 86
Anti-reflective coating 92
First metal layer 94
Conductive wiring 96
Second metal layer 108
Silicon oxide 118
Silicon nitride 119
Polyimide 120
Passivation layer 122
Dwg.2E/2

L12 ANSWER 2 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 2000-125679 [11] WPIX
DNN N2000-094694 DNC C2000-038161
TI **Insulative layer** etching method to provide an opening to a metal **bonding** pad of an **integrated circuit**.
DC G06 L03 P78 P84 U11
IN CHEN, F; CHEN, S; LEE, T; WU, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 6001538 A 19991214 (200011)* 8p
ADT US 6001538 A US 1998-55442 19980406
PRAI US 1998-55442 19980406
AB US 6001538 A UPAB: 20000301
NOVELTY - A silicon **wafer** (10) has a metal pad (16) over which is deposited a composite layer (20) comprising two **insulative layers**. A masking layer (22) is deposited over the **wafer** and is patterned to define an access opening (26) to the metal pad. The top **insulative layer** (20B) and a portion of the bottom **insulative layer** (20A) are isotropically etched in a plasma containing a first gas mixture. The remaining portion of the bottom **insulative layer** is anisotropically etched in a plasma containing a second gas mixture to expose the metal pad.
USE - For etching an **insulative layer** to provide an opening to a metal **bonding** pad of an **integrated circuit**.
ADVANTAGE - Provides an etched opening in a non-planarized **insulative layer** where the etch mask has thin regions without increasing the mask thickness to accommodate them. Allows openings to be etched in a non-planarized **insulative layer** with reduced photoresist thickness. Ensures that the photoresist layer suffers practically no erosion during the isotropic etch step so that the thin regions can then survive the reactive ion etching.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of an **integrated circuit wafer** showing a mask pattern on a **passivation** layer with a partially etched opening to a **bonding** pad after a first etching step.

Silicon **wafer** 10

Bonding pad 16

L14 ANSWER 1 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-302610 [34] WPIX
DNN N2002-236650 DNC C2002-088066
TI Dual damascene structure fabrication method on semiconductor **wafer**, involves forming photoresist layer on anti-reflecting layer, to define pattern of upper trench of dual damascene structure.
DC A85 L03 U11
IN HUANG, I; HUNG, K; HWANG, J
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6337269 B1 20020108 (200234)* 16p
ADT US 6337269 B1 US 2001-885042 20010621
PRAI US 2001-885042 20010621
AB US 6337269 B UPAB: 20020528

NOVELTY - An anti-reflecting layer is formed on **dielectric layer** (56) formed on a **passivation** layer (54). A photoresist layer is formed on the anti-reflecting layer, to define a pattern of an upper trench of the dual damascene structure.

The **dielectric layer** (56) and the **passivation** layer (54) are used as hard masks to perform an etching process for simultaneously forming positions of wiring lines and contact plugs.

DETAILED DESCRIPTION - A conductive layer (44) composed of a copper conductor is positioned on a substrate (42).

A **passivation** layer (46) composed of **silicon nitride**, silicon-oxy-nitride or silicon carbon, a **dielectric layer** (48) composed of low-K material which is consistent with parameters of FLARE, SiLK, **passivation layer** (50), **dielectric layer** (52), **passivation layer** (54) and **dielectric layer** (56) are sequentially formed on the substrate.

An anti-reflecting layer is formed on the **dielectric layer** (56).

A photoresist layer is formed on the anti-reflecting layer to define the pattern of the dual damascene structure.

The anti-reflecting **layer** and the **dielectric layer** (56) are etched according to the defined pattern and another anti-reflecting layer is formed on which another photoresist layer is formed to define a through-hole.

The **dielectric layer** (56) and the **passivation** layer (54) are used as hard masks to perform an etching process for simultaneously forming positions of wiring lines and contact plugs.

USE - For fabricating a dual damascene structure on a semiconductor **wafer** for manufacturing **integrated circuits** (**ICs**).

ADVANTAGE - The manufacturing process efficiency and the throughput are improved, since the problem of a residual photoresist layer in the bottom of the through-hole does not occur.

DESCRIPTION OF DRAWING(S) - The figure shows the dual damascene structure fabrication method.

Substrate 42
Conductive layer 44
Passivation layers 46,50,54
Dielectric layers 48,52,56
Dwg.13/20

L14 ANSWER 2 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-239118 [29] WPIX
CR 2001-564387 [59]; 2002-239065 [07]; 2002-239117 [09]; 2002-279612 [03]
DNN N2002-184378 DNC C2002-072042
TI Formation of dual-damascene type conducting interconnect for **microelectronics** fabrication, involves forming non-metallic barrier over trench and via, before forming metallic barrier and copper layer on exposed conducting layer.
DC A85 L03 U11
IN CHOOI, S; GUPTA, S; HONG, S; ZHOU, M
PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE
CYC 1
PI US 2002001952 A1 20020103 (200229)* 19p
ADT US 2002001952 A1 Div ex US 2000-512379 20000225, US 2001-925821 20010810
FDT US 2002001952 A1 Div ex US 6284657
PRAI US 2000-512379 20000225; US 2001-925821 20010810
AB US2002001952 A UPAB: 20020626
NOVELTY - A trench (22) and via (25) are patterned and etched through capping **layer** (20), **dielectric layer** (18), etch-stop **layer** (16), **dielectric layer** (14), extending to **passivating** layer (12).

A non-metallic barrier layer is formed over side walls of trench and via. The conducting layer (10) is exposed by etching layer (12). A metallic barrier layer is formed on trench and via and copper is deposited over it.

DETAILED DESCRIPTION - A trench and via are patterned and etched through capping **layer**, **dielectric layer** (18), etch-stop **layer**, **dielectric layer** (14), extending to **passivating** layer. A non-metallic layer is formed over all surfaces of trench and via formation such that non-metallic layer conformally covers the layers. The portions of non-metallic layer is etched to form a barrier spacer over the side walls of trench and via formation and the exposed portion of **passivation** layer is etched to expose the conducting layer. A metallic barrier layer is formed over trench and via formation and copper is deposited over trench and via formation.

USE - For formation of dual-damascene type conducting interconnects such as copper damascene type interconnects, in **microelectronics** fabrication.

ADVANTAGE - Diffusion of fluorine from fluorinated dielectric materials into metallic barrier layer is prevented, thereby protecting interconnect liner from adverse effects of fluorine. Similarly diffusion of conducting materials such as copper, deposited in trenches and vias into surrounding dielectric materials and sputtering onto side walls of trenches and vias during etching, are avoided. Copper interconnects of reduced dimensions required in devices of sub-micron (0.15 mu) generation, is offered. A lining layer with low-k dielectric properties is formed which reduces problems associated with parasitic capacitance between conducting interconnects and other neighboring structures. The lining layer has improved adhesion properties between conductors and porous dielectrics. A chemically inert spacer layer which protects surrounding materials from the effect of etches and post etched solvent stripping process, is formed.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of etched out trench and via of dual-damascene type interconnect.

Conducting layer 10
Passivating layer 12
Dielectric layers 14,18

Etch-stop layer 16
Capping layer 20
Trench 22
Via 25
Dwg.4/20

L14 ANSWER 3 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-239117 [29] WPIX
CR 2001-564387 [59]; 2002-239065 [07]; 2002-239118 [09]; 2002-279612 [03]
DNN N2002-184377 DNC C2002-072041
TI Formation of dual-damascene type conducting interconnect for **microelectronics** fabrication, involves forming non-metallic barrier over trench and via, before forming metallic barrier and copper layer on exposed conducting layer.
DC A85 L03 U11
IN CHOOI, S; GUPTA, S; HONG, S; ZHOU, M
PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE
CYC 1
PI US 2002001951 A1 20020103 (200229)* 19p
ADT US 2002001951 A1 Div ex US 2000-512379 20000225, US 2001-925820 20010810
FDT US 2002001951 A1 Div ex US 6284657
PRAI US 2000-512379 20000225; US 2001-925820 20010810
AB US2002001951 A UPAB: 20020626

NOVELTY - A trench (22) and via (25) are patterned and etched through capping **layer** (20), **dielectric layer** (18), etch-stop **layer** (16), **dielectric layer** (14), till **passivating** layer (12). A non-metallic barrier layer is formed over side walls of trench and via. The conducting layer (10) is exposed by etching layer (12). A metallic barrier layer is formed on trench and via, and copper is deposited over it.

DETAILED DESCRIPTION - A layered structure comprises conducting **layer**, **passivating layer**, **dielectric layer** (14), etch-stop **layer**, **dielectric layer** (18) and capping layer. A trench and via is patterned and etched on the layered structure extending till **passivating** layer. A non-metallic layer is formed over all surfaces of trench and via such that non-metallic layer con formally covers the layers. A portion of non-metallic layer is etched to form a barrier spacer over the side walls of trench and via, and the exposed portion of **passivating** layer is etched to expose the conducting layer. A metallic barrier layer is formed over all surfaces of trench and via, and copper is deposited over it.

USE - For formation of dual-damascene type conducting interconnects such as copper damascene type interconnects, in **microelectronics** fabrication.

ADVANTAGE - Diffusion of fluorine from fluorinated dielectric materials into metallic barrier layer is prevented, thereby protecting interconnect liner from adverse effects of fluorine. Similarly diffusion of conducting materials such as copper, deposited in trenches and vias into surrounding dielectric materials and sputtering onto side walls of trenches and vias during etching, are avoided. Copper interconnects of reduced dimensions required in devices of sub-micron (0.15 mu) generation, is offered. A lining layer with low-k dielectric properties is formed which reduces problems associated with parasitic capacitance between conducting interconnects and other neighboring structures. The lining layer has improved adhesion properties between conductors and porous dielectrics. A chemically inert spacer layer which protects surrounding materials from the effect of etches and post etched solvent stripping process, is formed.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of etched out trench and via of dual-damascene type interconnect.

Conducting layer 10
Passivating layer 12
Dielectric layers 14,18
Etch-stop layer 16
Capping layer 20
Trench 22
Via 25
Dwg.4/20

L14 ANSWER 4 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-239065 [29] WPIX
CR 2001-564387 [59]; 2002-239117 [09]; 2002-239118 [09]; 2002-279612 [03]
DNN N2002-184330 DNC C2002-072008
TI Formation of dual-damascene type conducting interconnect, used in **microelectronics**, involves covering surfaces of trench and via formation with non-metallic layer, metallic barrier layer and then with copper.
DC A85 L03 U11
IN CHOOI, S; GUPTA, S; HONG, S; ZHOU, M
PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE
CYC 1
PI US 2001055878 A1 20011227 (200229)* 19p
ADT US 2001055878 A1 Div ex US 2000-512379 20000225, US 2001-925822 20010810
FDT US 2001055878 A1 Div ex US 6284657
PRAI US 2000-512379 20000225; US 2001-925822 20010810
AB US2001055878 A UPAB: 20020626

NOVELTY - A dual-damascene type conducting interconnect is produced by:

(a) forming trench and via structure from a capping layer to a **passivating** layer;

(b) covering surfaces of the trench and via formation with non-metallic layer;

(c) forming a barrier on sidewalls of the trench and via formation; and

(d) covering all surfaces of the trench and via formation with metallic barrier layer, then with copper.

DETAILED DESCRIPTION - Formation of a dual-damascene type conducting interconnect involves:

(a) providing a layered structure comprising a conducting layer (10), a **passivating layer** (12), first **dielectric layer** (14), second **dielectric layer** (18) and a capping layer (20);

(b) patterning and etching a trench (22) and a via (25) structure passing through the capping layer, to the **passivating** layer;

(c) covering all surfaces of the trench and via formation with non-metallic layer;

(d) etching away portions of the non-metallic layer to form a barrier spacer on the side-walls of the trench and the via formation;

(e) etching away the exposed portion of the **passivation** layer to expose the conducting layer;

(f) covering all surfaces of the trench and via formation with metallic barrier layer; and

(g) covering all surfaces of the trench and via formation with copper.

USE - Formation of dual-damascene type conducting interconnects used in **microelectronic**.

ADVANTAGE - Provides interconnect structures that are impermeable to

fluorine and copper out-diffusions, and can be produced at reduced dimension, preferably sub-0.15 microns.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a dual-damascene type interconnect showing an etched out trench and via.

Conducting layer 10
Passivating layer 12
Dielectric layers 14, 18
Etch stop layer 16
Capping layer 20
Trench 22
Via 25
Dwg.4/20

L14 ANSWER 5 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-181554 [18] WPIX
DNN N2001-129470 DNC C2001-054105
TI Processing a semiconductor device for forming, e.g., charged-coupled devices, involves forming a protective film over the device, performing post processing, and selectively etching the protective film to expose the bond pads.
DC A85 L03 U11 U13
IN MICHAEL, J G; MILLER, J S; PITTMAN, G D; PREVITI-KELLY, R A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6174824 B1 20010116 (200118)* 7p
ADT US 6174824 B1 US 1999-262110 19990304
PRAI US 1999-262110 19990304
AB US 6174824 B UPAB: 20010402

NOVELTY - A semiconductor device is processed by (a) forming a protective film over the final **passivation** layer and the exposed bond pads of the semiconductor device, providing a semiconductor device assembly; (b) performing post processing of the semiconductor device assembly; and (c) selectively etching the protective film to expose the bond pads.

DETAILED DESCRIPTION - Processing a semiconductor device (100) by (a) forming a protective film over the final **passivation** layer and the exposed bond pads (120) of the semiconductor device, providing a semiconductor device assembly; (b) performing post processing of the semiconductor device assembly; and (c) selectively etching the protective film to expose the bond pads. The semiconductor device has metal level(s) (110), a final **passivation** layer protecting the metal level(s) and bond pads exposed through the final **passivation** layer for accessing the semiconductor device via the metal level(s).

USE - For post-processing a completed semiconductor device or **wafer** for forming, e.g., charged-coupled devices, integrated into the semiconductor device or **wafer**.

ADVANTAGE - The invention includes a protective film formed over the final **passivation** layer and exposed bond pads of the semiconductor device providing (a) bond pad protection on the post final **passivation** formation and etching; and (b) protection to the exposed bond pads from moisture and metallic migration, e.g., ionics. The method (a) is compatible with further semiconductor processing, (b) requires no special tools or process steps to implement the technique, (c) is a fast throughput film deposition process for the formation of the protective film, and (d) is cost effective.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor device assembly.

Semiconductor device 100
Metal level 110
Bond pads 120

Protective film 200
Post-process structures 300
Dwg.5/5

L14 ANSWER 6 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1999-419180 [35] WPIX
DNN N1999-312870 DNC C1999-123289
TI Formation of **passivation** structure.
DC A26 A85 L03 U11
IN BOHR, M T
PA (ITLC) INTEL CORP; (BOHR-I) BOHR M T
CYC 84
PI WO 9934442 A1 19990708 (199935)* EN 27p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
AU 9919172 A 19990719 (199951)
US 6143638 A 20001107 (200059)
KR 2001033663 A 20010425 (200164)
JP 2002500445 W 20020108 (200206) 27p
US 2002064929 A1 20020530 (200240)
ADT WO 9934442 A1 WO 1998-US26689 19981215; AU 9919172 A AU 1999-19172 19981215; US 6143638 A US 1997-1551 19971231; KR 2001033663 A KR 2000-707183 20000627; JP 2002500445 W WO 1998-US26689 19981215, JP 2000-526974 19981215; US 2002064929 A1 Div ex US 1997-1551 19971231, US 1998-115418 19980714
FDT AU 9919172 A Based on WO 9934442; JP 2002500445 W Based on WO 9934442
PRAI US 1997-1551 19971231; US 1998-115418 19980714
AB WO 9934442 A UPAB: 19990902
NOVELTY - A first dielectric and a conductive layer on a substrate are patterned to form a capped interconnect and bond pad. A second dielectric is formed between the capped interconnect and bond pad and a portion removed to expose them, and a third **dielectric layer** formed over the entire structure.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method where a hard mask is formed on a metal layer and patterned as above, followed by depositing and polishing of a low k dielectric constant material so that it is coplanar with the hard mask capped interconnect and bond pad, and a sealing **dielectric layer** formed over the entire structure.
USE - In semiconductor **integrated circuit** fabrication.
ADVANTAGE - A hermetic seal and low interconnect capacitance are achieved.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of an electrical contact on a bonding pad.
Bond pad 206
Sealing dielectric 216
Bond pad opening 220
Hard mask 224
Dwg.2i/2

L14 ANSWER 7 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1999-419176 [35] WPIX
DNN N1999-312866 DNC C1999-123288
TI **Wafer passivation** structure formation.

DC A85 L03 U11
IN BOHR, M T
PA (ITLC) INTEL CORP
CYC 82
PI WO 9934423 A1 19990708 (199935)* EN 25p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL
OA PT SD SE SZ UG ZW
W: AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH
GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK
MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US
UZ VN YU ZW
AU 9914109 A 19990719 (199951)
KR 2001033662 A 20010425 (200164)
JP 2002500440 W 20020108 (200206) 27p
ADT WO 9934423 A1 WO 1998-US24358 19981116; AU 9914109 A AU 1999-14109 19981116; KR 2001033662 A KR 2000-707182 20000627; JP 2002500440 W WO 1998-US24358 19981116, JP 2000-526962 19981116
FDT AU 9914109 A Based on WO 9934423; JP 2002500440 W Based on WO 9934423
PRAI US 1997-2178 19971231
AB WO 9934423 A UPAB: 19990902

NOVELTY - A first **dielectric layer** is formed over a metal interconnect layer including a bonding pad and a metal member spaced from the bonding pad by a gap, and a second **dielectric layer** over the first dielectric which is hermetic and has a larger dielectric constant.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (1) a method of hermetically sealing an **integrated circuit** by forming the **passivation** structure above, forming an opening through the **dielectric layers** to expose the top of the bonding pad, depositing a conducting barrier layer on the sides of the opening and on the top of the bond pad, and forming a bump on the barrier layer in the opening; (2) a method of forming a low interconnect capacitance **wafer** as above; and (3) a **passivation** film and a **passivation** structure formed by the above method.

USE - In semiconductor **integrated circuit** fabrication.

ADVANTAGE - A hermetic seal and low interconnect capacitance are achieved.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross section of a hermetic low capacitance structure.

Bond pads 204
Interconnects 206
Gaps 208
First dielectric 210
Sealing dielectric 212
Contact 215
Conductive barrier layer 216
Bump 218
Dwg.2/3

L14 ANSWER 8 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1998-466695 [40] WPIX
DNN N1998-363556 DNC C1998-141485
TI **Passivation** layer formation over spaced metal lines on semiconductor substrates - by sequentially forming plasma enhanced **silicon nitride**, silicon oxide and second **silicon nitride** layers.
DC A85 L03 P42 U11 X14

IN CHENG, Y; YU, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5795833 A 19980818 (199840)* 6p
ADT US 5795833 A US 1996-691080 19960801
PRAI US 1996-691080 19960801
AB US 5795833 A UPAB: 19981008

A method of making **passivation** layers over spaced metal lines (20) over a semiconductor structure comprises forming the metal lines having a height of 0.4-0.8 microns, a width of 0.5-1.5 microns and a spacing of 0.5-1.0 microns and forming a **silicon nitride** layer (24) 900-1000 Angstrom thick by plasma enhanced chemical vapour deposition) PECVD. This is followed by a **silica** layer (28) 4000-9000 Angstrom thick, formed by PECVD using a flow of O2, TEOS and N2, each at a flow rate of 900-1100 mg per minute, a pressure of 7.2-9.2 torr, a deposition temperature of 390-410 deg. C, an rf power of 650-775 W and an electrode gap of 220-280 mils.

A second **silicon nitride** layer (32), 4000-7000 Angstrom thick, is then formed by PECVD. Preferably an **insulating layer** of **polyimide** or epoxy is formed over the second nitride layer.

USE - In forming **passivation** layers over metal lines in semiconductor **integrated circuits**.

ADVANTAGE - The barrier is moisture-proof, step coverage is good and stress between the lines and overlying layers is reduced.

Dwg.2/2

L14 ANSWER 9 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1986-008453 [02] WPIX
DNN N1986-006066
TI **Integrated circuit** dielectric isolation forming system - is for semiconductor substrate and provides undercut **silica** isolation layer and recessed silicon sidewall arrangement.
DC U11
IN JAMBOTKAR, C G
PA (IBMC) IBM CORP
CYC 5
PI EP 166141 A 19860102 (198602)* DE 18p
R: DE FR GB
JP 61015344 A 19860123 (198610)
US 4663832 A 19870512 (198721)
EP 166141 B 19910410 (199115)
R: DE FR GB
DE 3582453 G 19910516 (199121)
ADT EP 166141 A EP 1985-105717 19850510; JP 61015344 A JP 1985-79461 19850416; US 4663832 A US 1984-626280 19840629
PRAI US 1984-626280 19840629
AB EP 166141 A UPAB: 19930922

A pattern of isolation trenches (18) is etched in the substrate using a mask pattern. The semiconductor body which establishes the trench is etched anisotropically to undercut the overlying mask pattern. An **insulating layer** of **silicon dioxide** (20) is provided by thermal oxidation of exposed silicon surfaces.

A **passivating** layer (15) of **silicon nitride** is formed over the trench surfaces and substrate to provide a continuous layer at an undercut of the mask. A second **insulating layer** (21) of **silicon dioxide** is formed over the nitride **passivating** layer and a **layer** (22) of **dielectric** is deposited over the

second layer, to fill the trench. The **dielectric layer** is etched back to the level of the second **insulating layer** in contact areas, which leaves a **dielectric layer** in the trench. The second **insulating layer** is etched uniformly to leave it only in the trench.

ADVANTAGE - A highly planar structure is achieved and the isolation trench exhibits improved insulation and **passivation** characteristics.

9/10

L14 ANSWER 10 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1989-283839 JAPIO
TI SEMICONDUCTOR DEVICE
IN KATO JURI
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 01283839 A 19891115 Heisei
AI JP1988-113019 (JP63113019 Heisei) 19880510
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 884, Vol. 14, No. 65, P. 24 (19900206)
AB PURPOSE: To prevent invasion of moisture into inside of an **IC** from the periphery of the **IC** clip so as to improve humidity resistance and elevate reliability by contacting, in a scribe area, an Si substrate or thermal **oxide film** on the Si substrate directly with **polyimide** resin formed at the upper layer.
CONSTITUTION: An ICAL pad 2 is formed on an Si substrate 1, which is covered with a **passivation** CVD **SiO2** 3 and CVD **Si3N4** and further covered with a **polyimide** film 5 in a scribe area 6, and there the **polyimide** 5 contacts directly with the Si substrate 1. Accordingly, moisture invading from the interface 11 is absorbed in the **polyimide** 5 having high hygroscopicity and does not permeate into the inside. Hereby, moisture and contaminant do not invade inside the **IC**. which realizes the product with high reliability.

L14 ANSWER 11 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1986-064171 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR ELEMENT
IN TAN SEIN TAN
PA YOKOGAWA HEWLETT PACKARD LTD, JP (CO 355232)
PI JP 61064171 A 19860402 Showa
AI JP1985-189322 (JP60189322 Showa) 19850828
PRAI US 1984-634250 19840905
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 426, Vol. 1, No. 228, P. 165 (19860808)
AB PURPOSE: To protect a semiconductor element from contamination generated during the treatment of a gate electrode region during the next treatment by operating a **dielectric layer** in a region between ohmic contact sections as a pre-**passivation** layer to a region on the semiconductor **wafer** to which a gate electrode is formed.
CONSTITUTION: An epitaxial layer 105, which has thickness of approximately 3,000.ANG. and is made of GaAs, is shaped onto a GaAs **wafer** 100. A **dielectric layer** 110, which has thickness of 2,000-4,000.ANG. and consists of **silicon dioxide**, is formed onto the epitaxial layer 105, and the **dielectric layer** 110 functions as a pre-**passivation** layer to a region, in which a gate electrode is shaped, in the GaAs **wafer**. The gate electrode region is protected during the next treatment period through the pre-**passivation**. Other substances, such as **silicon nitride**, **polyimide** or these mixture or

the like can also be used as the **dielectric layer** 110.

L18 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1992-284141 [34] WPIX
DNN N1992-217457 DNC C1992-126402
TI **IC bonding** pad structure with edge **passivation** - **silicon oxide-nitride** edge **coatings** prevent attack by contaminants and moisture-induced corrosion.
DC L03 U11
IN BYRNE, R C
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 1
PI US 5136364 A 19920804 (199234)* 4p
ADT US 5136364 A US 1991-713947 19910612
PRAI US 1991-713947 19910612
AB US 5136364 A UPAB: 19931006

A **die**-sealing **bonding** pad structure with edge **passivation** for an **IC bonding** pad includes a noble metal **bonding** face and sealed edges to protect from adverse environments and comprises an Al **bonding** pad on a semiconductor **IC**. A **passivation** layer (12) overlaps the edges only of the Al pad (11) and at least a barrier metal layer (15) and a noble metal outer layer (16) overlie the pad and overlap the **passivation** layer, with the barrier layer isolating the noble metal from the Al. A second **passivation** layer (17) overlaps the edges of the noble metal and barrier layers and seals their edges while the noble metal is exposed for the **IC** contact.

Pref. the noble metal is Au or Pt and the barrier metal is an alloy of Ti/W, Ni/V, Cr/Ni or Cr. Pref. there is an **adhesion** metal layer, pref. Al, between the **bonding** pad and barrier metal. Pref. the first and second **passivation** layers comprise at least a first **silica** layer, pref. a layer of Si nitride on the **silica**, and pref. the second **passivation** layer comprises a thick layer of low-melting glass or **insulating** organic material **coated** with Si nitride.

USE/ADVANTAGE - A **die**-sealing **bonding** pad (claimed) is provided which is useful for **ICs**. The **passivation** seal prevents attack by contaminants on the edges of the metallisation layers and stops moisture being drawn along the metal interfaces by capillary action and promoting corrosion.
3/5

L20 ANSWER 1 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-452941 [48] WPIX
DNN N2002-357081 DNC C2002-128772
TI **Integrated circuit chip passivation**
method involves sequentially forming three different dielectric layers
impermeable to moisture and exposing portion corresponding to **bond**
pad.
DC L03 U11
IN MOINPOUR, M; SCHATZ, K; SHIH, Y; SHUBERT, J V; WADA, G
PA (ITLC) INTEL CORP
CYC 1
PI US 6365521 B1 20020402 (200248)* 14p
ADT US 6365521 B1 US 1997-1265 19971231
PRAI US 1997-1265 19971231
AB US 6365521 B UPAB: 20020730
NOVELTY - A dielectric layer (120) which is impermeable to moisture, is deposited over the exposed surface of an **integrated circuit chip** including a **bond** pad (105).
Another dielectric layer (125) is deposited over the layer (120) to a thickness equivalent to the **bond** pad height. Another dielectric layer (130) which is impermeable to moisture is deposited over layer (125) after planarization, and portion of the **bond** pad is exposed.
USE - For **passivating integrated circuit chip**.
ADVANTAGE - The metal layers formed in **IC chip** are insulated with sufficient step coverage and are protected from environmental damage, particularly moisture by providing dielectric layers that are impermeable to moisture.
DESCRIPTION OF DRAWING(S) - The figure shows a planar side view of the **integrated circuit chip** structure.
Bond pad 105
Dielectric layers 120,125,130
Dwg.12/22

L20 ANSWER 2 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-402151 [43] WPIX
CR 2002-453955 [48]
DNN N2002-315297 DNC C2002-113168
TI Formation of top interconnection level and **bonding** pads of
integrated circuit involves forming wiring channels of
the top interconnection level by patterning trenches and vias in
insulative layer.
DC L03 U11
IN LIU, M; LIU, Y
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6358831 B1 20020319 (200243)* 13p
ADT US 6358831 B1 US 1999-261680 19990303
PRAI US 1999-261680 19990303
AB US 6358831 B UPAB: 20020730
NOVELTY - A top interconnection level and **bonding** pads of an **integrated circuit** are formed by forming wiring channels of the top interconnection level by patterning trenches and vias in an insulative layer.
DETAILED DESCRIPTION - Formation of a top interconnection level and **bonding** pads of an **integrated circuit**,
includes:

(a) providing a silicon **wafer** substrate (30) having **integrated circuit** devices and a first interconnection level;
(b) depositing an insulative layer (134) on the substrate;
(c) forming trenches and via openings to expose elements of the first interconnection level in the insulative layer;
(d) depositing a first layer of conductive material on the insulative layer;
(e) polishing the first layer of conductive material until the insulative layer is exposed, while leaving the conductive material in the trenches and the via openings, thus forming a second interconnection level containing conductive lines embedded in the insulative layer with segments to which **bonding** pads are to be directly connected;
(f) depositing an etch stop layer (56) on the substrate;
(g) patterning the etch stop layer to form openings (57, 64), each opening exposes one of the segments;
(h) depositing a second layer of conductive material (58) on the etch stop layer;
(i) patterning the second layer of conductive material to form a **bonding** pad (60) over each opening, thus forming **bonding** pads;
(j) depositing a **passivation** layer (62); and
(k) patterning and etching the **passivation** layer to form an access opening over each **bonding** pad. Each **bonding** pad is rectangular, and has planar length and width dimensions of 40-100 mu m. It extends over the etch stop layer, and is connected to a corresponding segment through a corresponding opening.

USE - For forming a top interconnection level and **bonding** pads of an **integrated circuit**.

ADVANTAGE - The method reduces the impact of environmental or other external electrical disturbances on the interconnection level. It forms the interconnection level without the occurrence of dishing of the **bonding** pads. It diminishes the risk of wire **bonding** damage to the interconnection level since the **bonding** pads lie above a top interconnection level. It eliminates the need for dummy **bonding** pads on the top interconnection level of a multilevel **integrated circuit**. The **bonding** pads are robust and flat, and have a thickness that is independent of the thickness of the interconnection level.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a top interconnection level and **bonding** pads.

Silicon **wafer** substrate 30
Etch stop layer 56
Openings 57, 64
Second layer of conductive material 58
Bonding pad 60
Passivation layer 62
Insulative layer 134
Dwg.6D/8

L20 ANSWER 3 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-253492 [30] WPIX
DNN N2002-195601 DNC C2002-075836
TI Laser accessible fuse formation in **integrated circuit** comprises etching laser access opening in two steps using transient etch stop layers to limit access opening depth after first step and finishing opening in second step.
DC L03 U11
IN CHEN, Y; TZENG, W; WANG, K

PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 6294474 B1 20010925 (200230)* 11p
ADT US 6294474 B1 US 1999-425906 19991025
PRAI US 1999-425906 19991025
AB US 6294474 B UPAB: 20020513

NOVELTY - A laser accessible fuse is formed in an **integrated circuit** by etching a laser access opening in two steps using a transient etch stop layers to limit the depth of the access opening after the first step and finishing the opening in the second step.

DETAILED DESCRIPTION - Formation of a laser accessible fuse in an **integrated circuit** involves:

(a) providing a silicon **wafer** (10) having **integrated circuit** devices and a first insulative layer;

(b) patterning a fusible material layer on the first insulative layer to form a fuse (18) with a rupture zone;

(c) depositing a silicon oxide layer on the **wafer**;

(d) patterning a polysilicon layer over the silicon oxide layer to form a first plate overlying the rupture zone;

(e) depositing a second insulative layer over the **wafer**;

(f) forming conductive contacts to the fuse on through openings in the second insulative layer and the silicon oxide layer, by which the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(g) patterning a first metal layer (34) having a super-adjacent first antireflective coating (ARC), on the second insulative layer to form a first inter-connective wiring level to the devices and the fuse, and a second plate, concentric with the first plate overlying the rupture zone;

(h) depositing a third insulative layer over the **wafer**;

(i) patterning the third insulative layer and penetrating first ARC, to form via openings and an access opening (46) which exposes the second plate;

(j) patterning a second metal layer (50) having a super-adjacent second ARC, on the third insulative layer to form **bonding** pads connected to the inter-connective wiring through vias in the third insulative layer, while simultaneously removing both the second metal layer and the second plate in the access opening;

(k) depositing a **passivation** layer (68) on the **wafer**;

(l) patterning the **passivation** layer and the ARC by anisotropically etching, with a first etchant gas mixture and a first silicon oxide-to-polysilicon selectivity, to expose the **bonding** pads and a region within the window opening, penetrating the third and second insulative layers, and stopping on the first plate; and

(m) after step (l), without breaking vacuum and with a second gas mixture and a second silicon oxide-to-polysilicon selectivity, etching through the first plate and partially into the second insulative layer, leaving a final thickness of the second insulative layer over the rupture zone.

USE - Forming a laser accessible fuse in an **integrated circuit**.

ADVANTAGE - The process provides improved control of dielectric thickness over the fuse. It also fits conveniently within the framework of an existing process and does not introduce any additional steps.

DESCRIPTION OF DRAWING(S) - The figure is a cross section of a portion of a Dynamic Random Access Memory **integrated circuit**.

Wafer 10
Fuse 18

First metal layer 34
Access opening 46
Second metal layer 50
Passivation layer 68
Dwg.1F/1

L20 ANSWER 4 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-253272 [30] WPIX
DNN N2002-195383 DNC C2002-075781
TI **Passivation** of **microelectronics** fabrication e.g. **integrated circuit**, by sequentially forming **microelectronics** layer, two dielectric layers, additional dielectric **passivation** layer, and polymer overcoat.
DC A85 L03 U11
IN FU, C; JANG, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6274514 B1 20010814 (200230)* 6p
ADT US 6274514 B1 US 1999-336807 19990621
PRAI US 1999-336807 19990621
AB US 6274514 B UPAB: 20020513

NOVELTY - A **microelectronics** fabrication is **passivated** by sequentially forming patterned **microelectronics** layer, two dielectric layers, additional silicon-containing dielectric **passivation** layer(s), and overcoating molded organic polymer layer. The dielectric layers are formed by high density plasma chemical vapor deposition.

DETAILED DESCRIPTION - **Passivating** a **microelectronics** fabrication comprises forming on a substrate (10) a patterned **microelectronics** layer (12a, 12b). A first dielectric layer (14a) is formed on the **microelectronics** layer by high density plasma chemical vapor deposition (HDP-CVD) employing a first deposition:sputtering ratio. A second dielectric layer (14b) is formed on the first dielectric layer by HDP-CVD employing a second deposition:sputtering ratio. Additional silicon-containing dielectric **passivation** layer(s) (16) is/are formed on the dielectric layer. An overcoating (20) molded organic polymer layer is formed on the **passivation** layer and substrate.

USE - For **integrated circuit**, charge coupled device, solar cell, radiation emitting diode, ceramics substrate, and flat panel display **microelectronics** fabrication (claimed).

ADVANTAGE - The method improves **adhesion** of molded organic polymer packaging structures to silicon-containing dielectric materials. The dielectric layers possess excellent physical and chemical properties with stability and freedom from undesirable impurities. The greater amount of surface topography, which occurs during formation of silicon-containing dielectric layers at high deposition:sputter rate ratios during HDP-CVD attenuates delamination and improves **adhesion** of the overlying layers. The formation of silicon-containing glass dielectric layers at low deposition:sputter rate ratios provides dielectric layers with better gap filling capability.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional diagram of a **microelectronics** fabrication.
Substrate 10
Microelectronics layer 12a, 12b
First dielectric layer 14a
Second dielectric layer 14b
Additional **passivation** layer 16
Polymer overcoating 20

Dwg.3/3

L20 ANSWER 5 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-579990 [65] WPIX
CR 2001-158865 [16]
DNN N2001-431799 DNC C2001-172069
TI **Integrated circuit** production on substrates, involves depositing dielectric layer on wiring layer, patterning, etching dielectric layer to form grid structures, depositing and patterning metal barrier layer.
DC A85 L03 U11
IN CHEN, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 2001016415 A1 20010823 (200165)* 11p
ADT US 2001016415 A1 Div ex US 1999-442497 19991118, US 2001-755282 20010108
FDT US 2001016415 A1 Div ex US 6191023
PRAI US 1999-442497 19991118; US 2001-755282 20010108
AB US2001016415 A UPAB: 20011108

NOVELTY - A metal wiring layer is embedded in an insulating layer which is provided on a substrate. A **passivating** dielectric layer is deposited on the metal wiring layer. The IMD is patterned and etched to form grid structures (6). A blanket of metal barrier layer is deposited. The metal barrier layer is patterned on the grid structures. A metal layer is deposited and patterned on the grid structures to form metal pad contact structures.

DETAILED DESCRIPTION - A substrate (1) having a layer of dielectric, inter-level dielectric (ILD), or an interconnect layer, or device contact region to P-N junctions, is provided. A first level of metal wiring (3) is embedded in a first layer of insulator (2). A blanket of **passivating** dielectric layer (IMD) is deposited on the first level metal wiring layer. The IMD is patterned and etched to form special interlocking grid structures with open contact regions to underlying first level metal wiring. A blanket of metal barrier layer (10) is deposited. The metal barrier layer is patterned on grid structures. A blanket of metal layer is deposited and patterned on grid structures to form metal pad contact structures. The process is repeated to construct multilevel pad structures by robust method to form metal pad contact structures for **chips**, **integrated circuits** and other applications.

An INDEPENDENT CLAIM is also included for **bond** pad structure which comprises a **passivating** layer and a barrier layer formed orderly on several conductive **bond** pads on a semiconductor substrate. The **passivating** layer has multiple openings to each **bond** pads. An upper surface of conductive pads provide improved **adhesion** for subsequently formed **bonds**
.

USE - For fabricating **integrated circuits** and other devices on substrates to form semiconductor **integrated circuit** devices.

ADVANTAGE - The robust unique metal pad interlocking structures with good **adhesion** properties, low thermal stress and good conductivity is formed easily and inexpensively in a short period of time by the new and improved method. The interlocking structure form islands of interlocking grid structures (an array in three dimensions) to enhance **adhesion** among the various layer of the metal stack pad structure for improved wire **bond** strength. The interlocking pad structure provides robust pad metal stack structures of high reliability. The unique contact pad structure provides thermal stress relief, improved wire

bond adhesion to the aluminum pad and prevents peeling during wire **bond adhesion** tests.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the deposition, patterning and defining of a thin barrier metal layer e.g. tantalum nitride on interlocking pad structures.

Substrate 1
Insulator 2
Metal wiring 3
Grid structures 6
Metal barrier layer 10
Dwg.2/4

L20 ANSWER 6 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-290381 [30] WPIX
DNN N2001-207453 DNC C2001-088902
TI Semiconductor device comprises first semiconductor layer(s) and second protecting layer comprising material with nano-crystalline and amorphous structure of specified crystalline grain size and resistivity.
DC L03 U11
IN BAKOWSKI, M; HARRIS, C; SZMIDT, J
PA (ACRE-N) ACREO AB
CYC 92
PI WO 2001020672 A1 20010322 (200130)* EN 24p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000038529 A 20010417 (200140)
EP 1214740 A1 20020619 (200240) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
ADT WO 2001020672 A1 WO 2000-SE505 20000315; AU 2000038529 A AU 2000-38529 20000315; EP 1214740 A1 EP 2000-917573 20000315, WO 2000-SE505 20000315
FDT AU 2000038529 A Based on WO 200120672; EP 1214740 A1 Based on WO 200120672
PRAI SE 1999-3242 19990913
AB WO 200120672 A UPAB: 20010603

NOVELTY - A semiconductor device comprises first semiconductor layer(s) and a second layer applied on at least a surface portion of the first layer for protecting the device. The protecting layer is of a second material having a nano-crystalline and amorphous structure composed of crystalline grains having a size less than 100 nm and a resistivity at room temperature exceeding 1 multiply 1010 Ohm cm.

DETAILED DESCRIPTION - A semiconductor device comprises first semiconductor layer(s) (2, 3) and a second layer applied on at least a surface portion of the first layer for protecting the device. The protecting layer is of a second material having a larger energy gap between the valence band and the conduction band than the first material forming the first layer. The second material has at least, in one portion of the protecting layer, a nano-crystalline and amorphous structure composed of crystalline grains having a size less than 100 nm and a resistivity at room temperature exceeding 1 multiply 1010 Ohm cm.

USE - None given.

ADVANTAGE - The device has a protecting layer that fulfills its function in a better way than layers already known; and to a large extent satisfies the demands put on such a layer, e.g., (a) good **adhesion** to the substrate (semiconductor layer), (b) structurally compatible with the substrate, (c) the properties are, as little as possible, dependent on

the temperature in the operational temperature range, (d) preserve high resistivity and high breakdown strength at high temperatures, (e) closely matched thermal expansion coefficients of the material of the semiconductor layer, (f) let the **grip** of the semiconductor layer go when the temperature changes, and be at least partially released, (g) mechanically, thermally, and chemically stable in the entire operational range of the device, (h) have a good thermal conduction, and (i) resistant to environmental influence.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of a portion of the device at the surface of a pn-junction.

First semiconductor layers 2, 3
First sub-layer 9
Second sub-layer 10
Dwg.2/4

L20 ANSWER 7 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-168046 [17] WPIX
DNN N2001-121187 DNC C2001-050065
TI Fabrication of multilayer **microelectronic** interconnect structure used in high density interconnects for high performance **microelectronic** device **chips** uses a low dielectric constant material, e.g. air as the intralevel dielectric.
DC A85 L03 U11 U14
IN BUCHWALTER, L P; CALLEGARI, A C; COHEN, S A; GRAHAM, T O; HUMMEL, J P; JAHNES, C V; PURUSHOTHAMAN, S; SAENGER, K L; SHAW, J M
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6184121 B1 20010206 (200117)* 18p
ADT US 6184121 B1 Provisional US 1997-52174P 19970710, US 1998-112919 19980709
PRAI US 1997-52174P 19970710; US 1998-112919 19980709
AB US 6184121 B UPAB: 20010328

NOVELTY - A multilayer **microelectronic** interconnect structure is fabricated by using a low dielectric constant material, e.g. air as the intralevel dielectric which reduces intralevel capacitance.

DETAILED DESCRIPTION - A multilayer **microelectronic** interconnect structure is fabricated by (i) applying a double layer thickness of a thermally stable and easily processable dielectric material (20, 30) having a top layer and a lower layer on a semiconductor **wafer** (10); (ii) patterning and etching trenches for wiring tracks on the top layer and vias in the lower layer; (iii) depositing a thin electrically conductive barrier/**adhesion** layer (60) in the trenches and vias and overfilling the trenches and vias with a thick conductive wiring layer metal; (iv) planarizing the wiring layer metal by etching or polishing to achieve a coplanar inlaid structure of conductors and vias embedded as metal features in the dielectric material; (v) repeating steps (i-iv) until a requisite number of wiring levels in the interconnect structure are fabricated; (vi) removing the dielectric metal from all areas of the **wafer** not directly covered by the conductors by means of an etching process while leaving the dielectric material intact under the metal feature; (vii) optionally applying a thin conformal **passivation** layer (100) to cap and protect the exposed metal features; (viii) annealing the etched structure at an elevated temperature in a reducing atmosphere to mitigate any plasma process induced damage; (ix) laminating a thin taut insulating cover layer (120) to the top surface of the **passivated** metal features; (x) optionally depositing a thin insulating environmental barrier layer (130) on top of the cover layer; (xi) etching terminal vias in the optional barrier layer, insulating cover layer, and the thin conformal **passivation** layer to provide access for terminal pad contacts; and

(xii) depositing and patterning terminal metal pads at the via locations to complete the interconnect structure.

USE - For use in high density interconnects for high performance **microelectronic** device **chips**, e.g. for logic, memory, communication, and microcontroller applications.

ADVANTAGE - The i structure possesses a very low capacitance and fast propagation speeds.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic sketch of the interconnect structure after terminal vias have been etched and terminal pads are deposited to complete the fabrication of the structure.

Semiconductor **wafer** 10
Double layer of dielectric material 20, 30
Thin electrically conductive barrier/**adhesion** layer 60
Thin conformal **passivation** layer 100
Thin taut insulating cover layer 120
Thin insulating environmental barrier layer 130

Dwg.4D/7

L20 ANSWER 8 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-158865 [16] WPIX
CR 2001-579990 [55]
DNN N2001-115774 DNC C2001-047094
TI **Integrated circuit** manufacture e.g. MOSFET devices etc., by pattering and etching **passivating** dielectric layer to form interlocking structures on which metal pad stack structure is formed.
DC A85 L03 U11 U12 U13
IN CHEN, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6191023 B1 20010220 (200116)* 10p
ADT US 6191023 B1 US 1999-442497 19991118
PRAI US 1999-442497 19991118
AB US 6191023 B UPAB: 20011113

NOVELTY - The method involves patterning and etching a blanket of **passivating** dielectric layer to form special interlocking grid structures with open contact regions to an underlying first level metal wiring. A metal barrier layer is then formed and patterned and defined. Metal pads are then formed repetitively to form multilevel pad structures to form metal pad contact structures for **chips** and **IC** 's.

DETAILED DESCRIPTION - Forming an **integrated circuit** (**IC**) and other devices on a substrate comprises:

(a) providing a substrate (1);
(b) forming an interlevel dielectric (ILD) layer over the substrate;
(c) providing a first level of metal wiring (3) defined and embedded in a first insulating layer (2) over the ILD;
(d) depositing a blanket of **passivating** dielectric (IMD) layer (4) over the first level of metal wiring;
(e) patterning and etching the IMD to form special interlocking grid structures (6) with open contact regions to the underlying first level metal wiring;
(f) depositing a blanket of a metal barrier (10) layer;
(g) patterning and defining the metal barrier layer;
(h) depositing a blanket of a metal layer (12) for forming metal pads on the interlocking grid structures;
(i) patterning and defining the metal pad layer to form the pads; and
(j) repeating the above steps to form multilevel pad structures to form metal pad contact structures for **chips** and **IC**'s.

USE - For forming interlocking metal pad structures used as lines,

vias and interconnect wiring for **chip** technology, **IC**
module technology and solid state devices requiring an integrated
electrical contact, MOSFET, CMOS, memory and logic devices (all claimed).
ADVANTAGE - The interlocking metal pad structures have good
adhesion, low thermal stress and good conductivity.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of a
device formed as above having the metal pad (stack) structure.
substrate 1
first insulator layer 2
first level metal wiring 3
IMD layer 4
interlocking structures 6
barrier metal layer 10
metal pad layer 12
Dwg.3/4

L20 ANSWER 9 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-040528 [05] WPIX
DNN N2001-030211 DNC C2001-011678
TI Formation of intermetal dielectric layer for a semiconductor **chip** comprises plasma treatment of thin insulator layer and dielectric layer and depositing thick insulator layer on the treated layers.
DC L03 U11
IN CHANG, C; JANG, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6153512 A 20001128 (200105)* 7p
ADT US 6153512 A US 1999-414922 19991012
PRAI US 1999-414922 19991012
AB US 6153512 A UPAB: 20010124
NOVELTY - Intermetal dielectric layer comprising thick insulator (8) and dielectric layer (6) having low dielectric constant (k) is produced by nitrogen or nitrogen oxide plasma treatments on the thin insulator and dielectric layer; and depositing a thick insulator layer on the treated layers.
DETAILED DESCRIPTION - Formation of an intermetal dielectric (IMD) layer on a substrate comprises:
(a) providing metal interconnect (3) structures overlying and contacting the underlying conductive structure (2);
(b) forming a thin insulator layer (4) on the metal structures;
(c) performing a first plasma treatment on the insulator layer (1);
(d) applying a low k dielectric layer consisting of hydrogen silsesquioxane (HSQ) or fluorinated silicon oxide (FSG) on the top surface (5) of the plasma treated layer;
(e) performing a second plasma treatment on the low k dielectric layer; and
(f) depositing a thick insulator layer on the treated low k layer to (roughened surface) (7) form a composite.
USE - The method is used for forming a low dielectric constant **passivating** layer used for semiconductor **chips**.
ADVANTAGE - The method improves the **adhesion** of a low k dielectric layer to a silicon oxide layer via nitrogen plasma treatments. The semiconductor produced has reduced capacitance and improved performance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a low k dielectric layer of the intermetal dielectric formed on an underlying thin silicon oxide layer.
Insulator layer 1, 4, 8
Conductive structure 2

Metal interconnect 3
Top surface 5
Dielectric layer 6
Roughened surface 7
Dwg.4/5

L20 ANSWER 10 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1999-517438 [43] WPIX
CR 1999-457679 [38]
DNN N1999-384709 DNC C1999-151060
TI Formation of bumped semiconductor device having trench for stress relief.
DC A85 L03 U11
IN KLEFFNER, J H; MISTRY, A B
PA (MOTI) MOTOROLA INC
CYC 1
PI US 5943597 A 19990824 (199943)* 5p
ADT US 5943597 A US 1998-94974 19980615
PRAI US 1998-94974 19980615
AB US 5943597 A UPAB: 19991020
NOVELTY - A trench is formed in a **passivation** layer. The trench surrounds a bump formed on a **bond** pad.
DETAILED DESCRIPTION - The method comprises
(i) forming a **passivation** layer (14) on a substrate (10) having a **bond** pad (12), a portion of the **passivation** layer overlying the **bond** pad,
(ii) patterning the **passivation** layer to form a trench (15), and
(iii) forming a bump (22) overlying the **bond** pad, the bump being surrounded by the trench.
USE - Manufacture of a bumped semiconductor device.
ADVANTAGE - The structure accommodates thermal and mechanical stress gradients by incorporation of a stress relief trench.
DESCRIPTION OF DRAWING(S) - The drawing shows a solder bump structure incorporating a stress isolation trench.
Semiconductor **die** 10
Bond pad 12
Passivation layer 14
Trench 15
Polyimide layer 16
Bump metallisation layer 18
Stud 20
Solder bump 22
Dwg.2/3

L20 ANSWER 11 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1994-266214 [33] WPIX
DNN N1994-209492 DNC C1994-121709
TI **Passivated IC** devices mfr. - in which the **IC** is protected by two **passivation** layers, pref. of ceramic, and exposed **bond** pads are protected by a barrier metal layer.
DC A85 L03 U11
IN MICHAEL, K W
PA (DOWO) DOW CORNING CORP
CYC 2
PI EP 613178 A2 19940831 (199433)* EN 9p
JP 07007101 A 19950110 (199511) 8p
EP 613178 A3 19941109 (199535)
US 5563102 A 19961008 (199646) 8p
ADT EP 613178 A2 EP 1994-301221 19940222; JP 07007101 A JP 1994-27821

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     19940225; EP 613178 A3 EP 1994-301221 19940222; US 5563102 A Div ex US
     1993-23450 19930226, US 1995-465286 19950605
PRAI US 1993-23450    19930226; US 1995-465286   19950605
AB   EP    613178 A UPAB: 19941010
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Method comprises: applying primary **passivation** (3) over the **IC** subassembly surface and **bond** pads (2); etching to expose the **bond** pads; applying a diffusion barrier metal layer (4) over the **bond** pads; adding overall sec. **passivation** (5); and etching to expose the barrier metal layer, pref. so that the sec. **passivation** covers the edges of the barrier metal layer.

ADVANTAGE - Structure is low cost and has improved performance and reliability.

Dwg.3/3

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L20  ANSWER 12 OF 17  WPIX (C) 2002 THOMSON DERWENT
AN   1993-271390 [34]   WPIX
DNN  N1993-208455        DNC C1993-121083
TI   Vacuum deposition of thin dielectric films for planar technology -
     includes adding oxygen to argon and nitrogen gas mixt. forming plasma.
DC   L03 M13 U11 U14
IN   DEGTEV, V E; GORIN, A V; KORNITSKII, E U
PA   (PLAT-R) PLATAN RES INST
CYC  1
PI   SU 1758085    A1 19920830 (199334)*       4p
ADT  SU 1758085 A1 SU 1990-4841109 19900712
PRAI SU 1990-4841109  19900712
AB   SU    1758085 A UPAB: 19931119
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This procedure involves sputtering a silicon target in a high frequency magnetron discharge plasma with a mixt. of ions of a gas contg. Ar and N2, and depositing the sputtered material onto a substrate. Oxygen is incorporated into the gas mixt., and the material is deposited at an Ar:N2:O2 gas ratio of 40:53:7 respectively. Films 0.1-0.3 microns thick can be deposited at a rate of 400-500 Angstrom/minute. Adding O2 to the mixt. (and thus to the film) and optimising the partial pressures ratio, increases **adhesion** and reduces the internal stresses.

USE/ADVANTAGE - In planar technology of prodn. of semiconductor devices for prepn. of **passivating** coatings in **integrated circuits**, dielectric films of thin-film electroluminescent structures, etc. A high quality dielectric coating from **silicon oxynitride** can be obtd. Bul.32/30.8.92

Dwg. 1/4

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L20  ANSWER 13 OF 17  WPIX (C) 2002 THOMSON DERWENT
AN   1992-270020 [33]   WPIX
DNN  N1992-206392        DNC C1992-120397
TI   Improved corrosion-resistant plastic encapsulated integrated
     circuit - having elastic insulating layer on top of the
     passivation layer of the side sealing round the ball and and
     preventing moisture ingress.
DC   A26 A85 L03 P73 U11
IN   ENDOH, T; HARADA, S; ISHIDA, T
PA   (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP; (MITQ)
     MITSUBISHI ELECTRIC KK
CYC  4
PI   DE 4201792     A  19920806 (199233)*      16p
     JP 04271132    A  19920928 (199245)       10p
     US 5430329     A  19950704 (199532)       16p
     DE 4201792     C2 19960515 (199624)       16p
     US 5525546     A  19960611 (199629)       14p
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KR 9602092 B1 19960210 (199909)
ADT DE 4201792 A DE 1992-4201792 19920123; JP 04271132 A JP 1991-9157 19910129; US 5430329 A Cont of US 1992-819739 19920113, Cont of US 1993-88597 19930709, US 1994-249679 19940526; DE 4201792 C2 DE 1992-4201792 19920123; US 5525546 A Cont of US 1992-819739 19920113, Cont of US 1993-88597 19930709, Div ex US 1994-249679 19940526, US 1995-416130 19950403; KR 9602092 B1 KR 1992-819 19920121
FDT US 5525546 A Div ex US 5430329
PRAI JP 1991-9157 19910129
AB DE 4201792 A UPAB: 19931025
The semiconductor device has one or more metallisation layers of which at least one (309, 310) has **bond** pads (6) for connection of **bond** wires to a lead frame. The metallisation layer (4), pref. Al, refractory metal, refractory metal - silicide or polycrystalline Si, is protected by a **passivation** layer (5), pref. Si oxide, Si nitride or **Si oxynitride**. In the **passivation** layer (5) a window (7) has been etched for an electrical contact by **bond** wire (24). The connection features at least near the **bond** pad and on the inner surface of the window (7) in the **passivation** layer an elastic insulating layer (10), pref. made of polyimide or silicone resin. The opening in the elastic layer is pref. inside the opening in the **passivation** layer. The opening may consist of multiple smaller openings.

USE/ADVANTAGE - The elastic layer can form a seal around the ball **bond** preventing moisture from reaching the metal layer inside the **bond** pad, where the **passivation** has been removed. The layer also cushions the pressure exerted on the **passivation** layer during the **bonding** operation, preventing cracking of this layer. As a result the reliability of the device, in terms of resistance to exposure to moisture, is improved. The method is used esp. for the assembly of **dice**, e.g. DRAMs or SRAMs, with large **bond** pad counts and those assembled by plastic moulding, forming thin packages.
1/12
ls
Dwg.1/12

L20 ANSWER 14 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1985-255926 [41] WPIX
DNN N1985-191482 DNC C1985-111001
TI Photochemical vapour deposition of **silicon oxynitride**
- using silicon, nitrogen and oxygen contg. gases to minimise free amorphous silicon in cpd..
DC E36 L03 P42 U11
IN PETERS, J W
PA (HUGA) HUGHES AIRCRAFT CO
CYC 9
PI US 4543271 A 19850924 (198541)* 8p
WO 8600651 A 19860130 (198606) EN
RW: DE FR GB IT NL SE
W: JP KR
EP 188438 A 19860730 (198631) EN
R: DE FR GB IT NL SE
JP 61502616 W 19861113 (198652)
EP 188438 B 19900627 (199026)
R: DE FR GB IT NL SE
DE 3578438 G 19900802 (199032)
KR 8903018 B 19890818 (199032)
JP 04008511 B 19920217 (199211) 8p
ADT US 4543271 A US 1984-627366 19840702; WO 8600651 A WO 1985-US728 19850422;

EP 188438 A EP 1985-902334 19850422; JP 61502616 W JP 1985-501924 19850422; JP 04008511 B JP 1985-501924 19850422

PRAI US 1984-627366 19840702

AB US 4543271 A UPAB: 19930925

A homogeneously chemically **bonded Si oxynitride** material contg. minimal free amorphous Si is deposited on a substrate surface by (a) placing the substrate in a photochemical vapour deposition chamber; (b) exposing the substrate to a vapour mixt. of (i) N-contg. cpd. and Si-contg. cpd. at flow rates and ratio for forming Si3N4; (ii) Hg vapour reaction sensitiser; and (iii) an O-contg. cpd. (c) simultaneously exposing the mixt. to radiation of a selected wavelength inducing a photochemical reaction between N-, Si- and O-contg. cpds. to form homogeneously **bonded Si oxynitride** which deposits on the substrate surface; where the amt. of O-contg. cpd. is sufficient to chemically **bond** excess Si and homogeneously incorporate it into the **Si oxynitride**, preventing formation and heterogenous incorporation of free amorphous Si in the cpd. The **Si oxynitride** so formed has a refractive index 1.7-1.8.

USE/ADVANTAGE - The **Si oxynitride** is useful as a **passivation** layer, insulating layer or mask in **IC** mfr. It has optimised physical and electrical properties, e.g. hardness, scratch resistance, **adhesion** and resistivity, better than conventional photochemically prepd. Si nitride which contains some amorphous Si.

1/2

L20 ANSWER 15 OF 17 JAPIO COPYRIGHT 2002 JPO
AN 1994-075244 JAPIO
TI SEMICONDUCTOR DEVICE
IN TAKAHASHI KUNIHIRO; KOJIMA YOSHIKAZU; TAKASU HIROAKI; YAMAZAKI TSUNEO; IWAKI TADAO
PA SEIKO INSTR INC, JP (CO 000232)
PI JP 06075244 A 19940318 Heisei
AI JP1992-220503 (JP04220503 Heisei) 19920819
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1756, Vol. 18, No. 321, P. 98 (19940617)
AB PURPOSE: To improve the reliability of a driving substrate for the active matrix- type light valve device formed by using an SOI substrate. CONSTITUTION: At least an **integrated circuit** is formed in a single crystal silicon layer 2 provided on an electrical insulator 1 in the semiconductor device. The **integrated circuit** is covered with a **passivation** film with a **silicon oxynitride** film or a silicon nitride film 3 as the uppermost layer. An **adhesive** layer 5 is formed on the **passivation** film, and the single crystal silicon layer 2 provided on the insulator 1 is **adhered** and fixed to a **holding** member 6 by the **adhesive** layer 5. The **integrated circuit** formed in the SOI substrate is transferred to the **holding** member 6 in this way, and a semiconductor device suitable to the driving substrate of a light valve device is obtained.

L20 ANSWER 16 OF 17 JAPIO COPYRIGHT 2002 JPO
AN 1991-280540 JAPIO
TI FORMING METHOD OF INSULATING FILM
IN HISAMUNE YOSHIAKI
PA NEC CORP, JP (CO 000423)
PI JP 03280540 A 19911211 Heisei
AI JP1990-82728 (JP02082728 Heisei) 19900329

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1178, Vol. 16, No. 1, P. 32 (19920313)

AB PURPOSE: To form a **silicon oxide nitride** film which is excellent in denseness and has high resistance to humidity, without damaging the surface of an object to be treated, by reacting organic silicon compound containing oxygen with ozone (O3), and performing chemical vapor deposition.

CONSTITUTION: A semiconductor **chip** 303 is mounted on an element mounting part 302 of a lead frame, and **bonded** to electrodes 304 by using **bonding** wires (gold wires) 305. In the last stage of a **wafer** process, a **passivation** film (silicon nitride film) 306 is formed by plasma CVD. The whole surface of the **chip** 303 is coated with a **silicon oxide nitride** (SixOyNz) film 307 together with outer leading-out parts 301 of the lead frame and the element mounting part 302. Said film 307 is formed at 250.degree.C by using triethyl silylamine oxide ((C2H5)3 SiNH2O) as organic silicon compound material and O3. Next, resin sealing, and the cutting and the shaping of a lead frame are performed, thereby completing a semiconductor device.

L20 ANSWER 17 OF 17 JAPIO COPYRIGHT 2002 JPO
AN 1989-025542 JAPIO
TI SEMICONDUCTOR DEVICE
IN KAGAMI TERUYUKI; MURAKAMI SUSUMU; SUGAWARA YOSHITAKA; FUKUDA TAKUYA; MOCHIZUKI YASUHIRO
PA HITACHI LTD, JP (CO 000510)
PI JP 01025542 A 19890127 Heisei
AI JP1987-181067 (JP62181067 Heisei) 19870722
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 759, Vol. 13, No. 213, P. 64 (19890518)

AB PURPOSE: To prevent poor breakdown strength and fluctuation in hFE due to increase in leaking current, by forming a **passivation** film having a specified dielectric constant .epsilon. by a .mu. wave plasma CVD method.

CONSTITUTION: A specified diffused layer is formed on an Si substrate 1 by an ordinary semiconductor process. Thus a semiconductor device is constituted. Then, thermal silicon oxide, which is a **passivation** film 2, and PSG are formed. A contact hole is provided. An Al electrode 3 is wired on the hole to a thick ness of 2.0.mu.m by a sputtering method. Thereafter, silicon nitride 4 having a dielectric constant .epsilon. of 5.9 or less is formed to a thickness of 2.0 .mu.m by a .mu.wave plasma CVD method. After a through hole is formed, annealing is performed with H2 at 450.degree.C. **Chips** are obtained by dicing. Wire **bonding** is performed. Sealing is performed with plastics 10 and the device is assembled. As the **passivation** film, any of phospho silicate glass (PSG) having a dielectric constant .epsilon. of 3.7 or less, silicon oxide of 3.9 or less and **silicon oxynitride** of 5.0 or less can be used.

L25 ANSWER 1 OF 5 WPIX (C) 2002 THOMSON DERWENT
AN 2002-237015 [29] WPIX
CR 2001-202099 [15]
DNN N2002-182323 DNC C2002-071685
TI **Integrated circuit** structure for creating aluminum wirebound pad on copper back-of-the-line, has **integrated circuit** semiconductor **wafer**, first and second **passivating** layers, barrier layer, and aluminum stack.
DC A85 L03 U11
IN COSTRINI, G; GOLDBLATT, R D; HEIDENREICH, J E; MCDEVITT, T L
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6333559 B1 20011225 (200229)* 10p
ADT US 6333559 B1 Div ex US 1998-167834 19981007, US 2000-487013 20000119
PRAI US 1998-167834 19981007; US 2000-487013 20000119
AB US 6333559 B UPAB: 20020508
NOVELTY - An **integrated circuit (IC)** structure comprises an **IC** semiconductor **wafer** having a copper wiring; a first **passivating** layer on top of the **wafer** having terminal via openings to expose the wiring; a barrier layer; an aluminum stack on the barrier layer; and a second **passivating** layer on the stack with openings that expose the stack covering the copper wiring.

DETAILED DESCRIPTION - An **integrated circuit** (**IC**) structure contains an aluminum (Al) contact (40) in electrical communication with an underlying copper (Cu) wiring; a first **passivating** layer on top of the **wafer** having terminal via openings (26) to expose the Cu wiring; a barrier layer on at least the exposed Cu wiring, sidewalls of the terminal via openings, and on the **passivating** layer near the terminal via openings; an Al stack on the barrier layer; and a second **passivating** layer on the Al stack having openings that expose the Al stack covering the Cu wiring.

USE - For creating an aluminum wirebound pad on a copper back-of-the-line (beol).

ADVANTAGE - The structure significantly reduces the Cu wiring from exposure or environmental attack, and eliminates the problem associated with Cu-Al intermixing.

DESCRIPTION OF DRAWING(S) - The figures show top views of two types of structures.

Terminal via openings 26
Al contact 40
Dwg.5/5

L25 ANSWER 2 OF 5 WPIX (C) 2002 THOMSON DERWENT
AN 2002-224202 [28] WPIX
DNN N2002-171668 DNC C2002-068395
TI Packaging and testing semiconductor package includes depositing polymer film over **passivation** layer and over metal lines.
DC A85 L03 S01 U11
IN CHIEN, W; CHU, H; YIU, H
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 6274397 B1 20010814 (200228)* 5p
ADT US 6274397 B1 US 1999-323351 19990601
PRAI US 1999-323351 19990601
AB US 6274397 B UPAB: 20020502
NOVELTY - A semiconductor package is protected and tested by depositing a **passivation** layer (16) over the circuit elements (10, 14) without

covering the metal lines (18); depositing a polymer film (30) over the **passivation** layer and the metal lines; removing the polymer film; testing the package for line corrosion; depositing a layer of molding compound (40); and testing the package for line corrosion.

USE - For protecting and testing a semiconductor package.

ADVANTAGE - By depositing the polymer film, the exposed metal lines are protected against corrosion over a period of weeks or even months. Thus, the semiconductor package remains in a dormant or storage stage for as long as required.

DESCRIPTION OF DRAWING(S) - The figures are cross-sections of the **IC** after the deposition of the polymer film and of the molding compound.

Circuit elements 10, 14
Passivation layer 16
Metal lines 18
Polymer film 30
Molding compound 40
Dwg.2, 4/4

L25 ANSWER 3 OF 5 WPIX (C) 2002 THOMSON DERWENT
AN 2001-202099 [20] WPIX
CR 2002-237015 [23]
DNN N2001-144122 DNC C2001-059969
TI Forming an aluminum contact electrically connected with copper wiring in an **integrated circuit** comprises forming aluminum stack on barrier layer and patterning and etching stack and barrier layer.
DC L03 U11
IN COSTRINI, G; GOLDBLATT, R D; HEIDENREICH, J E; MCDEVITT, T L
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 3
PI US 6187680 B1 20010213 (200120)* 10p
KR 2000028654 A 20000525 (200120)
TW 404038 A 20000901 (200120)
ADT US 6187680 B1 US 1998-167834 19981007; KR 2000028654 A KR 1999-38815 19990911; TW 404038 A TW 1999-102628 19990223
PRAI US 1998-167834 19981007
AB US 6187680 B UPAB: 20020508

NOVELTY - Forming an aluminum contact electrically connected with copper wiring comprises forming, in sequence, a **passivating** layer, terminal via openings, barrier layer and aluminum stack on an **integrated circuit** semiconductor **wafer** having an embedded copper wiring; patterning and etching aluminum stack and barrier layer; and forming second **passivating** layer and openings.

DETAILED DESCRIPTION - Forming an aluminum (Al) contact electrically connected with copper (Cu) wiring (22) comprises forming a **passivating** layer (24) on an **integrated circuit** (**IC**) semiconductor **wafer** (20) having an embedded Cu wiring. Terminal via openings are formed through the **passivating** layer to expose the Cu wiring. A barrier layer (28) is formed at least over the exposed Cu wiring, on the side walls of the terminal via openings and on regions of the barrier layer near the terminal via openings. An Al stack (30) is formed on the barrier layer at least in the terminal via openings and on regions of the barrier layer near the terminal via openings. The Al stack and the barrier layer are patterned and etched. A second **passivating** layer (32) is formed over the patterned Al stack. Second openings are provided in the second **passivating** layer to expose regions of the patterned Al stack on top of the Cu wiring.

USE - For forming an aluminum contact electrically connected with

2001-646957 [25]; 2002-129435 [76]; 2002-402153 [34]
DNN N1998-189225 DNC C1998-074669
TI Solder bump formation on semiconductor **chips** to facilitate flip **chip** attachment to a substrate - by forming a via in a **passivation** layer, metallization, and then physical polishing to remove excess metallization.
DC A85 L03 U11 V04
IN AKRAM, S
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5736456 A 19980407 (199821)* 22p
ADT US 5736456 A CIP of US 1996-612059 19960307, US 1996-682141 19960717
PRAI US 1996-682141 19960717; US 1996-612059 19960307
AB US 5736456 A UPAB: 20020709
A fabrication method for under bump metallization on a semiconductor substrate comprises; (a) covering a semiconductor substrate in a **passivation** layer (56); (b) forming at least one via (62) for external contact, through the **passivation** layer to provide access to the underlying semiconductor (54); (c) forming a conformal metal layer (68, 70, 72) over the **passivation** layer where the metal layer is thinner than the **passivation** layer and where the metallization extends down into the via and contacts the semiconductor; and (d) removing the metallization covering the **passivation** layer by abrasion (78) to leave the metallization layer in the via only. Also claimed is a process in which a conductive element on a semiconductor substrate may be relocated by first covering the semiconductor with a **passivation** layer, topped by a metal layer with a contact point through the **passivation** later to the semiconductor below and then performing steps (a)-(d) above on the metal layer at a location different to the point at which the metal layer contacts the semiconductor thus providing a relocated semiconductor connection point.

Preferably the abrasion is carried out using chemical mechanical polishing. The **passivation** layer (56) may be **silicon dioxide**, **silicon nitride**, or a **polyimide** layer.

USE - In connecting **microelectronic chips** to carrier substrates, e.g. printed circuit boards using ball grid array (BGA) solder balls, or slightly larger than **integrated circuit** carrier (SLICC) techniques.

ADVANTAGE - The process requires fewer processing steps to form solder bumps than prior art processes thus increasing process efficiency.
Dwg.3a,3b/8

US 1001310304P1

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